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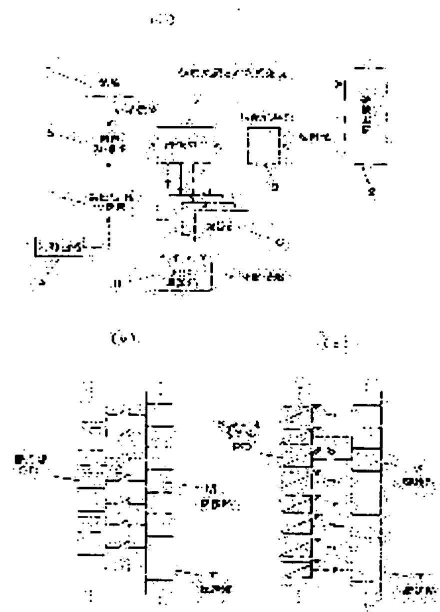
(54) RANGE FINDER AND RANGE-FINDING METHOD USING IMAGING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To contrive a control method for a general CCD imaging element to realize an operation substantially equivalent to synchronous integration, and to realize inexpensive light wave range-finding, which requires an imaging element of specified structure in the prior art, using the general CCD imaging element.
SOLUTION: This range finder is constituted to have an imaging element 4 arrayed one-dimensionally or two-dimensionally with a plurality of photo-sensitive parts on a semiconductor substrate, and having structure capable of controlling sensitivity in each of the photo-sensitive parts by impressing a voltage to the semiconductor substrate, and to have a sensitivity control part 5 synchronized with a modulation signal for intensity-modulated light to impress the voltage for modulating the sensitivity of the each photo-sensitive part to the semiconductor substrate of the imaging element 4. The sensitivity of the each photo-sensitive part is able to get variable synchronized with the intensity-modulated irradiation light, and the light wave range-finding is realized thereby.



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CLAIMS

[Claim(s)]
[Claim 1]
Distance measuring equipment using the image sensor characterized by having the sensibility control section which impresses the electrical potential difference which makes the semi-conductor substrate of said image sensor modulate the sensibility of each of said sensitization section synchronizing with the modulating signal of the light by which intensity modulation was carried out on the semi-conductor substrate in two or more sensitization sections with-dimensional [1] or the image sensor which is arranged two-dimensional and has controllable structure for the sensibility of each of said sensitization section by electrical-potential-difference impression to said semi-conductor substrate.
[Claim 2]
The image sensor which has the structure where of-dimensional [1] or the transfer section which reads stored charge from the are-recording section of each sensor element while arranging two-dimensional can be formed in said semi-conductor substrate for a sensor element equipped with the sensitization section which makes a signal charge generate according to light income, and the are-recording section which accumulates the signal charge generated in the sensitization section on a semi-conductor substrate, and the sensibility of the sensitization section can be substantially reduced by electrical-potential-difference impression to said semi-conductor substrate,
Image formation optical system to which the field where the sensor element of said image sensor was arranged carries out image formation of the reflected light from the detected material irradiated by the light by which intensity modulation was carried out,
The sensibility control section which impresses the control voltage for reducing the sensibility of said sensitization section to said semi-conductor substrate synchronizing with the modulating signal of said light by which intensity modulation was carried out,
The storage section which reads the charge accumulated in the are recording section of said image sensor covering two or more periods of said intensity modulation by said transfer section, and is memorized as measured value,
The detection phase setting section which changes the phase of the low sensibility period when the control voltage for reducing the sensibility of said sensitization section among round terms of said intensity modulation is impressed whenever measured value is memorized by said storage section,

Distance measuring equipment using the image sensor characterized by having the ranging operation part which calculates the distance information to a detected material for every sensor element based on two or more measured value from which the phase of the low sensibility period memorized by the storage section differs.
[Claim 3]
While arranging a sensor element equipped with the sensitization section which makes a signal charge generate according to light income, and the are recording section which accumulates the signal charge generated in the sensitization section two-dimensional on a semi-conductor substrate The transfer section which reads stored charge from the are recording section of each sensor element is formed in said semi-conductor substrate. By impressing a high electrical potential difference which breaks down the potential barrier of the sensitization section in the direction perpendicular to the front face of said semi-conductor substrate It is the ranging approach using the INTARAIN transfer-die CCD image sensor which has a vertical mold overflow drain electrode for discarding the signal charge of the sensitization section to said semi-conductor substrate,
In the condition that the field where the sensor element of said image sensor was arranged carries out image formation of the reflected light from the detected material irradiated by the light by which intensity modulation was carried out It synchronizes with the modulating signal of said light by which intensity modulation was carried out. The 1st phase which repeats the actuation which impresses the control voltage for making said semi-conductor substrate discard the signal charge of said sensitization section to said vertical mold overflow drain electrode covering two or more periods of said intensity modulation in a predetermined period among round terms of said intensity modulation,
The 2nd phase read by said transfer section by making into measured value the charge accumulated in the are recording section of said image sensor in the 1st phase,
The 3rd phase which changes the phase of the period which impresses said control voltage to said vertical mold overflow drain electrode in the 1st phase whenever measured value is read in the 2nd phase,
The ranging approach using the image sensor characterized by having the 4th phase of calculating the distance information to a detected material for every sensor element, based on two or more measured value from which the phase of the period which impresses said control voltage differs after repeating the 1st, 2nd, and 3rd phase two or more times.
[Claim 4]
While arranging a sensor element equipped with the sensitization section which makes a signal charge generate according to light income, and the are recording section which accumulates the signal charge generated in the sensitization section two-dimensional on a semi-conductor substrate The transfer section which reads stored charge from the are recording section of each sensor element is formed in said semi-conductor substrate. By impressing a high electrical potential difference which breaks down the potential barrier of the sensitization section in the direction level on the front face of said semi-conductor substrate It is the ranging approach using the INTARAIN transfer-die CCD image sensor which has a horizontal-type overflow drain electrode for discarding the signal charge of the sensitization section in the direction level on the front face of said semi-conductor substrate,
In the condition that the field where the sensor element of said image sensor was arranged carries out image formation of the reflected light from the detected material irradiated by the light by which intensity modulation was carried out The 1st phase which repeats the actuation which impresses the control voltage for making the signal charge of said sensitization section discard in a predetermined period among round terms of said intensity modulation to said horizontal-type overflow drain electrode synchronizing with the modulating signal of said light by which intensity modulation was carried out covering two or more periods of said intensity modulation,
The 2nd phase read by said transfer section by making into measured value the charge accumulated in the are recording section of said image sensor in the 1st phase,
The 3rd phase which changes the phase of the period which impresses said control voltage to

said horizontal-type overflow drain electrode in the 1st phase whenever measured value is read in the 2nd phase,
The ranging approach using the image sensor characterized by having the 4th phase of calculating the distance information to a detected material for every sensor element, based on two or more measured value from which the phase of the period which impresses said control voltage differs after repeating the 1st, 2nd, and 3rd phase two or more times.
[Claim 5]
It has the three or more sensitization sections which make a signal charge generate according to light income, respectively. The image pick-up section which arranges the sensor element which accumulated the signal charge two-dimensional on a semi-conductor substrate, and grows into said specific sensitization section by giving potential which brings a signal charge together in the specific sensitization section except both ends from other sensitization sections, The transfer section which reads stored charge from each sensor element of the image pick-up section is formed in said semi-conductor substrate. It is the ranging approach using the frame transfer-die CCD image sensor which has a vertical mold overflow drain electrode for discarding the signal charge of the sensitization section to said semi-conductor substrate by impressing a high electrical potential difference which breaks down the potential barrier of the sensitization section in the direction perpendicular to the front face of said semi-conductor substrate,
In the condition that the field where the sensor element of said image sensor was arranged carries out image formation of the reflected light from the detected material irradiated by the light by which intensity modulation was carried out It synchronizes with the modulating signal of said light by which intensity modulation was carried out. It has left the signal charge accumulated in said specific sensitization section among the three or more sensitization sections which constitute said each sensor element from a predetermined period among round terms of said intensity modulation. The 1st phase which repeats the actuation which impresses control voltage which makes said semi-conductor substrate discard the signal charge of other sensitization sections to said vertical mold overflow drain electrode covering two or more periods of said intensity modulation,
The 2nd phase read by said transfer section by making into measured value the charge accumulated in said specific sensitization section of each of said sensor element in the 1st phase,
The 3rd phase which changes the phase of the period which impresses said control voltage to said vertical mold overflow drain electrode in the 1st phase whenever measured value is read in the 2nd phase,
The ranging approach using the image sensor characterized by having the 4th phase of calculating the distance information to a detected material for every sensor element, based on two or more measured value from which the phase of the period which impresses said control voltage differs after repeating the 1st, 2nd, and 3rd phase two or more times.
[Claim 6]
It has the three or more sensitization sections which make a signal charge generate according to light income, respectively. The image pick-up section which arranges the sensor element which accumulated the signal charge two-dimensional on a semi-conductor substrate, and grows into said specific sensitization section by giving potential which brings a signal charge together in the specific sensitization section except both ends from other sensitization sections, The transfer section which reads stored charge from each sensor element of the image pick-up section is formed in said semi-conductor substrate. It is the ranging approach using the frame transfer-die CCD image sensor which has a horizontal-type overflow drain electrode for discarding the signal charge of the sensitization section by impressing a high electrical potential difference which breaks down the potential barrier of the sensitization section in the direction level on the front face of said semi-conductor substrate,
In the condition that the field where the sensor element of said image sensor was arranged carries out image formation of the reflected light from the detected material irradiated by the light by which intensity modulation was carried out It synchronizes with the modulating signal of said light by which intensity modulation was carried out. It has left the signal charge accumulated

in said specific sensitization section among the three or more sensitization sections which constitute said each sensor element from a predetermined period among round terms of said intensity modulation. The 1st phase which repeats the actuation which impresses control voltage which makes the signal charge of other sensitization sections discard to said horizontal-type overflow drain electrode covering two or more periods of said intensity modulation,
The 2nd phase read by said transfer section by making into measured value the charge accumulated in said specific sensitization section of each of said sensor element in the 1st phase,
The 3rd phase which changes the phase of the period which impresses said control voltage to said horizontal-type overflow drain electrode in the 1st phase whenever measured value is read in the 2nd phase,
The ranging approach using the image sensor characterized by having the 4th phase of calculating the distance information to a detected material for every sensor element, based on two or more measured value from which the phase of the period which impresses said control voltage differs after repeating the 1st, 2nd, and 3rd phase two or more times.
[Claim 7]
In claims 5 or 6, the sensitization section which constitutes said each sensor element consists of four or more. In the period which makes the signal charge of others and the sensitization section discard with the signal charge left accumulated in said specific sensitization section The ranging approach using the image sensor characterized by impressing the electrical potential difference which forms a potential barrier which isolates said specific sensitization section electrically from other sensitization sections in the sensitization section which adjoins said specific sensitization section.
[Claim 8]
The ranging approach using the image sensor characterized by forming the protection-from-light section in the front face of said specific sensitization section and the sensitization section in which said potential barrier is formed in claim 7.
[Claim 9]
The sensitization section which makes a signal charge generate according to light income, and the are recording section which accumulates the signal charge generated in the sensitization section, While arranging a sensor element equipped with the electric switch which opens and closes migration of the signal charge from the sensitization section to the are recording section on-dimensional [1] or a two-dimensional target on a semi-conductor substrate The image sensor which has the structure forms in said semi-conductor substrate the transfer section which reads stored charge from the are recording section of each sensor element, and said electric switch can be opened and closed by the RF by electrical-potential-difference impression to the specific electrode of said semi-conductor substrate,
Image formation optical system to which the field where the sensor element of said image sensor was arranged carries out image formation of the reflected light from the detected material irradiated by the light by which intensity modulation was carried out,
The synchronous integral control section which impresses the control voltage for closing said electric switch to said specific electrode of said semi-conductor substrate synchronizing with the modulating signal of said light by which intensity modulation was carried out, and the storage section which reads the charge accumulated in the are recording section of said image sensor covering two or more periods of said intensity modulation by said transfer section, and is memorized as measured value,
The detection phase setting section which changes the phase of the synchronous integral period when the control voltage for closing said electric switch among round terms of said intensity modulation is impressed whenever measured value is memorized by said storage section,
Distance measuring equipment using the image sensor characterized by having the ranging operation part which calculates the distance information to a detected material for every sensor element based on two or more measured value from which the phase of the synchronous integral period memorized by the storage section differs.
[Claim 10]

While constituting said transfer section by forming the transfer electrode for carrying out a sequential transfer in the front face of said are recording section in claim 9 at the are recording section which adjoins the signal charge accumulated in said are recording section In the period when the electrical potential difference for transmitting a signal charge is not impressed to said transfer electrode By impressing by turns the electrical potential difference which makes the signal charge generated in said sensitization section in said transfer electrode transport to said are recording section, and the electrical potential difference which does not make the signal charge which occurred in said sensitization section transport to said are recording section Distance measuring equipment using the image sensor characterized by constituting the electric switch which opens and closes migration of the signal charge from said sensitization section to the are recording section by high frequency.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
This invention relates to the technique which detects the delay of the phase of the reflected light to exposure light for every pixel of an image sensor, and makes the spacial configuration of a detected material detectable about the distance measuring equipment and the ranging approach of having used the image sensor.
[0002]
[Description of the Prior Art]
Drawing 3 is the principle explanatory view of the electro-optical distance measurement of the conventional TOF (Time Of Flight) method. For one, as for a detected material and 3, the light source and 2 are [image formation optical system and 4] image sensors among drawing. The light source 1 consists of LED arrays, and intensity modulation of the output light is carried out by the RF. Two or more LED is used for the light source 1 for increasing output luminous intensity, and each LED is synchronizing and emitting light. When intensity modulation of the light irradiated by the detected material 2 from the light source 1 is carried out by the RF which is 20MHz, since the wavelength is set to 15m, if light goes and comes back to the distance which is 7.5m, the delay of the phase of one period will produce it.
[0003]
Drawing 4 explains the delay of the phase of the reflected light to exposure light. Among drawing, W is the reflected light and the phase lag of psi has produced exposure light and R in the reflected light. If the reflected light R is sampled 4 times about one period of the exposure light W and the detection value of the reflected light in case the phases of exposure light are 0 degree, 90 degrees, 180 degrees, and 270 degrees is made into A0, A1, A2, and A3, respectively, delay psi of a phase will be given by the degree type.
Psi=arctan {(A3-A1) /(A0-A2)}

[0004]
Image formation of the light reflected by the detected material 2 is carried out to the light-receiving side of an image sensor 4 through the image formation optical system 3. Two or more pixels (X, Y) are arranged two-dimensional in the light-receiving side of an image sensor 4, and the three-dimensional structure of a detected material 2 can be detected by asking for phase lag psi (X, Y) by the upper type about each pixel.
[0005]
The sampling of multiple times must be able to do the image sensor used for the electro-optical distance measurement of this TOF method about one period of exposure light, and drawing 5 or structure like drawing 6 is conventionally proposed by Patent Publication Heisei No. 508736 [ten to]. The image sensor of drawing 5 is equipped with the one sensitization section PD and four memory cells M0, M1, M2, and M3 about 1 pixel, and the electric switches S0, S1, S2, and S3 turned on in time sharing are formed between each memory cells M0, M1, M2, and M3 and the sensitization section PD. Each electric switches S0, S1, S2, and S3 are turned on in T0, T1 and T2 of drawing 4 , and the period of T3, respectively. By repeating this actuation over two or more rounds, the S/N ratio to a dark current noise, a shot noise (noise by generating dispersion of an electronic-electron hole pair), the stationary noise of an amplifier circuit, etc. can be raised, and the detection values A0, A1, and A2 of the reflected light and A3 are accumulated in memory cells M0, M1, M2, and M3. Such actuation is carried out to calling it a "synchronous integral." The image sensor of drawing 6 is equipped with the shift register SR for data read-out, a light-receiving signal is accumulated in each memory cells M0, M1, M2, and M3 of a shift register SR from the one sensitization section PD through four electric switches S0, S1, S2, and S3 turned on in time sharing, and a light-receiving signal is read by the transfer facility of a shift register SR.
[0006]
[Problem(s) to be Solved by the Invention]
However, in manufacturing specially the image sensor which has special structure as shown in above-mentioned drawing 5 or above-mentioned drawing 6 , a manufacturing cost becomes high and the cost of the whole distance measuring equipment goes up. Then, it found out that the actuation same with carrying out the synchronous integral substantially was realizable by controlling skillfully the electrical potential difference impressed to the overflow drain electrode or perpendicular transfer electrode of a CCD image sensor by devising the control approach of a general CCD image sensor when it examines whether a synchronous integral is unrealizable.
[0007]
This invention is made based on such knowledge, is devising the control approach of a general CCD image sensor, makes realizable actuation same with carrying out the synchronous integral substantially, and makes it a technical problem to realize cheaply electro-optical distance measurement which needed the image sensor of special structure conventionally using a general CCD image sensor.
[0008]
[Means for Solving the Problem]
In order that the distance measuring equipment of this invention may solve the above-mentioned technical problem, as shown in drawing 1 Two or more sensitization sections on a semi-conductor substrate-dimensional [1] or the image sensor 4 which is arranged two-dimensional and has controllable structure for the sensibility of each of said sensitization section by electrical-potential-difference impression to said semi-conductor substrate, It is characterized by having the sensibility control section 5 which impresses the electrical potential difference which makes the semi-conductor substrate of said image sensor 4 modulate the sensibility of each of said sensitization section synchronizing with the modulating signal of the light by which intensity modulation was carried out. The image formation optical system 3 to which the field where the sensor element of an image sensor 4 was arranged carries out image formation of the reflected light from the detected material 2 more specifically irradiated by the light by which intensity modulation was carried out, The sensibility control section 5 which impresses the control voltage for reducing the sensibility of the sensitization section of an image sensor 4 to

the semi-conductor substrate of an image sensor 4 synchronizing with the modulating signal of said light by which intensity modulation was carried out, The storage section 6 which reads the charge accumulated in the are recording section of said image sensor 4 covering two or more periods of said intensity modulation by the transfer section, and is memorized as measured value, The detection phase setting section 7 which changes the phase of the low sensibility period when the control voltage for reducing the sensibility of the sensitization section among round terms of said intensity modulation is impressed whenever measured value is memorized by said storage section 6, It is characterized by having the ranging operation part 8 which calculates the distance information to a detected material 2 for every sensor element of an image sensor 4 based on two or more measured value from which the phase of the low sensibility period memorized by the storage section 6 differs.

[0009]

The image sensor 4 used for the distance measuring equipment of this invention here The sensitization section PD which makes a signal charge generate according to light income as shown in drawing 1 (b) While arranging a sensor element equipped with electric switch S which opens and closes migration of the signal charge to the are recording section M on-dimensional [1] or a two-dimensional target on a semi-conductor substrate from the are recording section M which accumulates the signal charge generated in the sensitization section PD, and the sensitization section PD The transfer section T which reads stored charge from the are recording section M of each sensor element is formed in said semi-conductor substrate. [whether it considers as the image sensor which has the structure which can open and close said electric switch S by the RF by electrical-potential-difference impression to the specific electrode (for example, transfer electrode) of said semi-conductor substrate, and] Or although said electric switch S cannot be opened and closed by the RF as shown in drawing 1 (c), turning this ON It considers as an image sensor which has sensibility adjustable sensitization section PD' which can make sensibility fluctuate by the RF by electrical-potential-difference impression to other specific electrodes (for example, overflow drain electrode) of said semi-conductor substrate. The frame transfer-die CCD image sensor which specifically has the INTARAIN transfer-die CCD image sensor which has a vertical mold or a horizontal-type overflow drain electrode, a vertical mold, or a horizontal-type overflow drain electrode, or the frame INTARAIN transfer-die CCD image sensor which is these compound dies can be used.

[0010]

Drawing 2 is the explanatory view of this invention of operation. Among drawing, (a) shows the phase of the exposure light W and (b) - (e) shows the detection phase for the synchronous integral set up in the detection phase setting section 7. The one sensitization section PD, two or more switches S0-S3, and two or more memory cells M0-M3 were formed, and switches S0, S1, S2, and S3 were made to turn on in time sharing for every sensor element, in a Prior art, with the detection phase of drawing 2 (b), (c), (d), and (e), respectively, as shown in drawing 5 or drawing 6 . The sensitization section PD which makes a signal charge generate in this invention according to light income for every sensor element as shown in drawing 1 (b) It has every one electric switch S which opens and closes migration of the signal charge to the are recording section M from the are recording section M which accumulates the signal charge generated in the sensitization section PD, and the sensitization section PD. By repeating and turning on electric switch S with the detection phase of drawing 2 (b) at the time of the 1st image pick-up, the measured value equivalent to A0 of drawing 4 is obtained in the are recording section M, and this is read to it by one screen by the transfer section T. By repeating and turning on electric switch S with the detection phase of drawing 2 (c), (d), and (e), respectively at the time of the 2nd time, the 3rd time, and the 4th image pick-up, the measured value equivalent to A1 and A2 of drawing 4 , and A3 is obtained in the are recording section M, and this is read to it by one every screen and the transfer section T. Generalization control of the above actuation is carried out by the control circuit 9. If it does in this way, although the 4 times as many measuring time as this will be required compared with the case where the image sensor of the structure shown in drawing 5 or drawing 6 is used, if a detected material 2 does not move at high speed, the image of four sheets with which detection phases differ is acquirable, and even if it uses a

general CCD image sensor, electro-optical distance measurement is realizable. In addition, the ranging operation part 8 can constitute a microcomputer, DSP, an operational amplifier, etc. from a means of arbitration that what is necessary is just what can calculate distance information substantially.

[0011]

By the way, in the CCD image sensor of the most general INTARAIN transfer die as a CCD image sensor, since the electrode which constitutes electric switch S of drawing 1 (b) is used also [electrode / perpendicular transfer] and this electrode was formed through the insulating thin film on the semi-conductor substrate, considering the configuration, electrostatic capacity was large, and when capacity was large, it turned out that it is very difficult to open and close by the dozens of MHz RF. In such a case, it is unsuitable for the application which realizes electro-optical distance measurement of a short distance using a general CCD image sensor.

[0012]

Then, as shown in drawing 1 (c), it examined whether electric switch S between the sensitization section and the are recording section would have a means by which only the sensibility of the sensitization section can be periodically reduced synchronizing with exposure light, maintaining in the ON condition. Since the sensibility of the sensitization section is a thing [as opposed to / a thing / light income] of the generating effectiveness of a photoelectron in short, if some generated photoelectrons can be thrown away, sensibility will fall substantially.

[0013]

As a means to throw away the photoelectron of such the sensitization section, some which have the structure called the overflow drain for throwing away a superfluous signal charge into a substrate are in a CCD image sensor. Although this overflow drain is formed in order to throw away the signal charge which exceeds predetermined level in order for the generated superfluous signal charge to prevent affecting the surrounding sensitization section, when the light which is too strong in the sensitization section also in a basis receives into a substrate If this overflow drain lowers intentionally the level which makes a signal charge overflow, even if the signal charge of the sensitization section is not superfluous, a signal charge will be thrown away as a superfluous thing and can reduce the sensibility of the sensitization section substantially. And since this overflow drain is directly linked with the substrate, considering a configuration, electrostatic capacity is small and switching by dozens of MHz is also possible. So, in the phase which does not want to detect light, if an overflow drain sets up low the level which makes a signal charge overflow, the sensibility of the sensitization section can be modulated according to the period of exposure light.

[0014]

Of course, although the view of using this overflow drain electrode for the electronic shutter of a CCD camera existed from the former, since it meant exposure of the end once, it was what starts an integral from the condition that the charge of the are recording section was initialized. The control approach that applied-voltage control of an overflow drain electrode realizes exposure of multiple times, with the after-image by exposure to last time left is not learned without initializing the charge of the are recording section.

[0015]

Hereafter, the concrete control approach for realizing the actuation same about the INTARAIN transfer-die CCD image sensor and frame transfer-die CCD image sensor which have a vertical mold or a horizontal-type overflow drain electrode as a synchronous integral is explained in detail as a gestalt of implementation of invention.

[0016]

[Embodiment of the Invention]

(Gestalt 1 of operation)

Drawing 7 shows the configuration of INTARAIN transfer-die CCD (IT-CCD) which has a vertical mold overflow drain (VOD) electrode. It is formed in the front face of n mold substrate 10 so that the vertical mold overflow drain (VOD) electrode 11 which consists of an aluminum electrode may contact a substrate directly without an insulator layer. Control voltage Vs is impressed to the VOD electrode 11. p mold field 12 is formed in the part surrounded with the VOD electrode

11 of the front face of n mold substrate 10. Two or more photodiodes are separated and formed in this p mold field 12. The part described as PD is a photodiode among drawing, and front faces other than the part in which this photodiode PD was formed are covered by the light-shielding film (not shown). Although the photodiode PD of four lines is perpendicularly illustrated horizontally three trains in drawing 7 , many photodiodes PD are formed more in fact. each -- a photodiode -- PD -- adjoining -- forming -- having had -- an electrode -- a -- b -- c -- d -- and -- a -- ' -- b -- ' -- c -- ' -- d -- ' -- perpendicular -- a transfer -- CCD -- an electrode -- it is -- this -- an electrode -- the bottom -- a photodiode -- PD -- having generated -- a signal charge -- accumulating -- accumulating -- having had -- a signal charge -- the perpendicular transfer electrical potential differences V1, V2, V3, and V4 of four phases -- the level transfer CCD -- transmitting . (The electrode of the perpendicular transfer CCD which adjoined the photodiode PD of each train and was formed is connected through wiring which is not illustrated so that the same perpendicular transfer electrical potential difference as the electrode horizontally located in a line may be impressed.) level -- a transfer -- CCD -- two -- phases -- level -- a transfer -- an electrical potential difference -- VH -- one -- VH -- two -- a charge -- transmitting -- a sake -- level -- a transfer -- an electrode -- e -- f -- e -- ' -- f -- ' -- e -- " -- f -- " -- having -- **** . In IT-CCD, it is very common for 4 phase clock to perform a perpendicular transfer and to perform a level transfer with 2 phase clock, and since it is the thing of the common knowledge about the structure of the charge transfer, detailed explanation is omitted.

[0017]

Drawing 8 shows the cross-section structure of the parts of Photodiode PD and the perpendicular transfer electrodes a and b. As mentioned above, p mold field 12 is formed in the front face of n mold substrate 10, and two or more photodiodes PD are formed in the front face of this p mold field 12. Each photodiode PD consists of an n+ field 13 and a p mold field 12. The p+ layer 14 is formed in the front face of Photodiode PD. If the effectiveness of this p+ layer 14 is explained, crystallinity will be bad and will be one with the bad (energy is activity) stability of energy, it is easy to generate an electronic-electron hole pair by thermal excitation, and this will serve as the dark current and the crystal structure on the front face of a substrate will serve as a cause which worsens the S/N ratio of a signal charge. In order to prevent this effect, it is the role of the p+ layer 14 to make it a signal charge not pass along near a front face, and the photodiode which has this structure is called the embedding photodiode etc. Each photodiode PD is adjoined and n layer 15 which constitutes the perpendicular transfer CCD is formed in the front face of p mold field 12. In this front face of n layer 15, it is SiO2. The perpendicular transfer electrodes a and b which consist of a polish recon gate electrode are formed through the becoming insulating thin film 16. Since this polish recon gate electrode is formed through the insulating thin film 16, electrostatic capacity is large considering a configuration, and when electrostatic capacity is large, it is difficult [it] to switch by dozens of MHz high frequency. In addition, the cross-section structure of the parts of Photodiode PD and the perpendicular transfer electrodes c and d is the same as that of drawing 8 .

[0018]

Drawing 9 shows the cross-section structure of the perpendicular transfer electrodes a, b, c, and d of the perpendicular transfer CCD about the A-A' line of drawing 8 . The 1st perpendicular transfer electrode a and c plays charge read-out to the perpendicular transfer CCD, and the role of a perpendicular transfer from Photodiode PD. The 2nd perpendicular transfer electrode b and d plays the role of a perpendicular transfer. The light-shielding film 17 is formed in the upper part of the perpendicular transfer electrodes a, b, c, and d.

[0019]

Drawing 10 shows electronic potential along with the thick broken line of drawing 8 . That is, along with p+ layer 14' (strictly formed at another process in the p+ layer 14 on the front face of a substrate), and the n+ layer 13 of Photodiode PD, p mold field 12 and n mold substrate 10, electronic potential is shown from n layer 15 of the perpendicular transfer CCD. Photodiode PD and the potential barrier (the broken line on the right-hand side of drawing 10 shows) of the p+ layer 14 during the perpendicular transfer CCD can be broken down by making high applied

voltage of the perpendicular transfer electrodes a and c. Moreover, the potential barrier (the broken line on the left-hand side of drawing 10 shows) of p mold field 12 between Photodiode PD and n mold substrate 10 can be broken down by making applied voltage of the VOD electrode 11 high. What gave the notation of − (minus) to the white round head in drawing means the photoelectron. Moreover, what gave a pattern like a "mane" to the perimeter with the photoelectron of the part of Photodiode PD means the photoelectron generated by photo electric conversion. Also in the following explanation, it is the same.

[0020]

When a light very strong against Photodiode PD carries out incidence of the original reason for having prepared the VOD electrode in IT-CCD, it is for missing a superfluous signal charge to n mold substrate 10, but in this invention, even if a signal charge is not superfluous, it makes sensibility of Photodiode PD adjustable by making it superfluous [a signal charge] and making a substrate overflow to lower the sensibility of Photodiode PD. That is, when the sensibility of Photodiode PD wants to fall, he lowers the potential barrier of p mold field 12 between the n+ layer 13 of Photodiode PD, and n mold substrate 10, and is trying to miss the generating charge of Photodiode PD to n mold substrate 10 by impressing high + electrical potential difference to the VOD electrode 11. Although the potential barrier of p+ layer 14' exists also between Photodiode PD and the perpendicular transfer CCD, the charge which lowered the potential barrier of p+ layer 14', and was generated in Photodiode PD can be brought together in the bottom of the perpendicular transfer electrode a by impressing predetermined + electrical potential difference to the 1st perpendicular transfer electrode a. When high + electrical potential difference is impressed to the VOD electrode 11, although the charge generated with Photodiode PD flows to the perpendicular transfer CCD, since a few will be thrown away into the direction of n mold substrate 10 with electronic potential low mainly comparatively for it by it, the sensibility (photoelectric conversion efficiency) of Photodiode PD falls substantially. Let this photoelectron abandonment period be a synchronous integral idle period (non-detecting phase). Moreover, when the applied voltage of the VOD electrode 11 is reduced and abandonment of a photoelectron is stopped, the charge generated with Photodiode PD will flow efficiently to the perpendicular transfer CCD, and will be accumulated in the bottom of a perpendicular transfer electrode. Let this photoelectron are recording period be a synchronous integral period (detection phase).

[0021]

Actuation of each period of are recording of the photoelectron by VOD mold IT-CCD, abandonment, and read-out is shown and explained to drawing 11 . In the are recording period of a photoelectron, the applied voltage of the VOD electrode 11 is low, and the sufficiently high electrical potential difference V1 is given to the perpendicular transfer electrode a currently formed next to Photodiode PD, and as shown in drawing 11 (a), the potential barrier by p+ layer 14' under a perpendicular transfer electrode currently formed between 15 and the n+ layer 13 n layers while lowering n layers of potentials of 15 is broken down. This is equivalent to electric switch S of drawing 1 (c) having closed. In this case, the photoelectron generated in the n+ layer 13 is accumulated in n layer 15 under a perpendicular transfer electrode.

[0022]

In the abandonment period of a photoelectron, the high + electrical potential difference Vs is impressed to the VOD electrode 11 connected to n mold substrate 10, and the potential of n mold substrate 10 is lowered. When applied voltage Vs is sufficiently high, as shown in drawing 11 (b), the potential barrier by p mold field 12 formed between n mold substrate 10 and the n+ layer 13 collapses, and many of photoelectrons generated in the n+ layer 13 are discarded by n mold substrate 10. At this time, an electrical potential difference V1 is kept impressed to the perpendicular transfer electrode a like the are recording period of a photoelectron. This is equivalent to what electric switch S of drawing 1 (c) has closed. If the applied voltage Vs of the VOD electrode 11 is set up so that the potential of n mold substrate 10 may become low rather than the potential of 15 n layers, since the photoelectron under a perpendicular transfer electrode generated in the n+ layer 13 can be drawn near to the one where potential is lower, most is discarded to the VOD electrode 11 (n mold substrate 10), without going to the

perpendicular transfer electrode a side. Moreover, since the photoelectron under a perpendicular transfer electrode accumulated in 15 n layers has the potential barrier of the n+ layer 13 during the are recording period of a photoelectron, it is not discarded at the VOD electrode 11 (n mold substrate 10) side.
[0023]
Alternation of the are recording period (drawing 11 (a)) of a photoelectron and the abandonment period (drawing 11 (b)) of a photoelectron is carried out within a round term of exposure light, for example, they accumulate a photoelectron only with a specific detection phase (synchronous integral period) like drawing 2 (b), and discard a photoelectron in the remaining non-detecting phase (integral idle period) (the photoelectron of the are recording section is generated in the sensitization section, left). By repeating this actuation covering two or more periods of exposure light, the detection value equivalent to A0 of drawing 4 is acquired for every pixel. This detection value is read for a while.
[0024]
In the read-out period of the accumulated photoelectron, as shown in drawing 11 (c), the electrical potential difference V1 of the perpendicular transfer electrode a is set up low, the transfer clock of four phases is given to the transfer electrical potential differences V1-V4, and the accumulated signal charge is read so that n layers of potential barriers by p+ layer 14' of the perpendicular transfer CCD may be generated between 15 and the n+ layer 13 of Photodiode PD. This is equivalent to the condition that electric switch S of drawing 1 (b) opened.
[0025]
Thus, if the detection value equivalent to A0 of drawing 4 is acquired for every pixel next, the detection value equivalent to A1 of drawing 4 will be acquired for every pixel by shifting a detection phase 90 degrees and repeating are recording and abandonment of a photoelectron like drawing 2 (c), covering two or more periods of exposure light. If this detection value is read, the detection value equivalent to A2 of drawing 4 and A3 will be shortly acquired for every pixel drawing 2 (d) and by shifting a detection phase like 180 degrees and 270 degrees, going, and repeating are recording and abandonment of a photoelectron still like drawing 2 (e), covering two or more periods of exposure light. In addition, the count of the synchronous integral of each time does not have making it the same also until it says it.
[0026]
The sequence which shifts a detection phase is not limited above. for example, formula [of a ranging operation]: -- psi=arctan {(A3-A1) /(A0-A2)} -- doubling -- the beginning -- the detection value of A3 -- asking -- the 1st image memory -- accumulating -- a degree -- the detection value of A1 -- asking (A3-A1) -- the 1st same image memory is overwritten. next, the detection value of A0 -- asking -- the 2nd image memory -- accumulating -- further -- the detection value of A2 -- asking (A0-A2) -- the 2nd same image memory is overwritten. Thus, if it carries out, the storage capacity of an image memory can be managed with one half.
[0027]
Moreover, a detection phase may make a detection phase large, in order not to necessarily consider as the narrow period when it was restricted in a round term like drawing 2 (b) - (e) and to raise a S/N ratio. For example, it can also acquire far and near information that the 1st image which measured a detection phase and the remaining one half for the one half in a round term as a non-detecting phase, and this 1st image compare the 2nd image which replaced and measured the detection phase and the non-detecting phase.
[0028]
Furthermore, about the exposure light by which intensity modulation was carried out, the amplitude does not need to be a sine wave, and it does not matter even if intensity modulation is carried out by the square wave or the triangular wave, either.
Moreover, the exposure light by which intensity modulation was carried out does not need to be the light, and can be used for the near infrared which is not visible, then the monitor application of Nighttime, etc.
[0029]
by the way, since CCD which has a vertical mold overflow drain electrode cannot carry out until

formation of the n+ field of Photodiode PD deeply while it can enlarge light-receiving area of Photodiode PD, it has the fault to which the sensibility to a near infrared becomes low. then, in order to cancel this fault, IT-CCD which has the horizontal-type overflow drain (LOD) electrode which can carry out until formation of the n+ field of Photodiode PD deeply is explained below.

[0030]

(Gestalt 2 of operation)

Drawing 12 shows the configuration of INTARAIN transfer-die CCD (IT-CCD) which has a horizontal-type overflow drain (LOD). Two or more n mold fields 20 are perpendicularly formed in the front face of p mold substrate 22, and the n mold each field 20 is connected to the LOD electrode 21 which consists of an aluminum electrode. Control voltage Vs is impressed to the LOD electrode 21. The n mold each field 20 is adjoined, and two or more photodiodes are separated and formed in the front face of p mold substrate 22. The part described as PD is a photodiode among drawing, and front faces other than the part in which this photodiode PD was formed are covered by the light-shielding film. Although the photodiode PD of four lines is perpendicularly illustrated horizontally three trains in drawing 12 , many photodiodes PD are formed more in fact. each -- a photodiode -- PD -- adjoining -- forming -- having had -- an electrode -- a -- b -- c -- d -- and -- a -- ' -- b -- ' -- c -- ' -- d -- ' -- perpendicular -- a transfer -- CCD -- an electrode -- it is -- this -- an electrode -- the bottom -- a photodiode -- PD -- having generated -- a signal charge -- accumulating -- accumulating -- having had -- a signal charge -- the perpendicular transfer electrical potential differences V1, V2, V3, and V4 of four phases -- the level transfer CCD -- transmitting . (The electrode of the perpendicular transfer CCD which adjoined the photodiode PD of each train and was formed is connected through wiring which is not illustrated so that the same perpendicular transfer electrical potential difference as the electrode horizontally located in a line may be impressed.) level -- a transfer -- CCD -- two -- phases -- level -- a transfer -- an electrical potential difference -- VH -- one -- VH -- two -- a charge -- transmitting -- a sake -- level -- a transfer -- an electrode -- e -- f -- e -- ' -- f -- ' -- e -- " -- f -- " -- having -- **** . In IT-CCD, it is very common for 4 phase clock to perform a perpendicular transfer and to perform a level transfer with 2 phase clock, and since it is the thing of the common knowledge about the structure of the charge transfer, detailed explanation is omitted.

[0031]

Drawing 13 shows the surrounding cross-section structure of Photodiode PD and the perpendicular transfer electrodes a and b. As mentioned above, n mold field 20 connected to the LOD electrode 21 is formed in the front face of p mold substrate 22, this n mold field 20 is adjoined and Photodiode PD is formed. Each photodiode PD consists of an n+ field 23 and a p mold substrate 22. The p+ layer 24 is formed in the front face of Photodiode PD. If the effectiveness of this p+ layer 24 is explained, crystallinity will be bad and will be one with the bad (energy is activity) stability of energy, it is easy to generate an electronic-electron hole pair by thermal excitation, and this will serve as the dark current and the crystal structure on the front face of a substrate will serve as a cause which worsens the S/N ratio of a signal charge. In order to prevent this effect, it is the role of the p+ layer 24 to make it a signal charge not pass along near a front face, and the photodiode which has this structure is called the embedding photodiode etc. Each photodiode PD is adjoined and n layer 25 which constitutes the perpendicular transfer CCD is formed in the front face of p mold substrate 22. In this front face of n layer 25, it is SiO2. The perpendicular transfer electrodes a and b which consist of a polish recon gate electrode are formed through the becoming insulating thin film 26. Since this polish recon gate electrode is formed through the insulating thin film 26, electrostatic capacity is large considering a configuration, and when electrostatic capacity is large, it is difficult [it] to switch by dozens of MHz high frequency. In addition, the surrounding cross-section structure of Photodiode PD and the perpendicular transfer electrodes c and d is the same as that of drawing 13 .

[0032]

The cross-section structure about the A-A' line of drawing 13 is the same as drawing 9 . The 1st perpendicular transfer electrode a and c plays charge read-out to the perpendicular transfer

CCD, and the role of a perpendicular transfer from Photodiode PD. The 2nd perpendicular transfer electrode b and d plays the role of a perpendicular transfer. The light-shielding film 27 is formed in the upper part of the perpendicular transfer electrodes a, b, c, and d. Moreover, the light-shielding film 27 is formed also in the upper part of n mold field 20 connected to the LOD electrode 21.

[0033]

Drawing 14 shows electronic potential along with the thick broken line of drawing 13 . that is, -- perpendicular -- a transfer -- CCD -- n -- a layer -- 25 -- from -- p -- + -- a layer -- 24 -- ' (strictly formed at another process in the p+ layer 24 on the front face of a substrate) -- a photodiode -- PD -- n -- + -- a layer -- 23 -- p -- + -- a layer -- 24 -- ' -- LOD -- an electrode -- 21 -- connecting -- having had -- n -- a mold -- a field -- 20 -- meeting -- electronic potential -- being shown . Photodiode PD and the potential barrier (the broken line on the right-hand side of drawing 14 shows) of p+ layer 24' during the perpendicular transfer CCD can be broken down by making high applied voltage of the perpendicular transfer electrodes a and c. Moreover, the potential barrier (the broken line on the left-hand side of drawing 14 shows) of p+ layer 24' between Photodiode PD and n mold field 20 can be broken down by making applied voltage of the LOD electrode 21 high.

[0034]

Although it is for missing a superfluous signal charge to n mold field 20 contiguous to Photodiode PD in IT-CCD of a LOD mold when a light very strong against Photodiode PD carries out incidence of the original reason for having prepared the LOD electrode In this invention, even if a signal charge is not superfluous, sensibility of Photodiode PD is made adjustable by making it superfluous [a signal charge] and making n mold field 20 overflow to lower the sensibility of Photodiode PD. That is, when the sensibility of Photodiode PD wants to fall, he lowers the potential barrier of p+ layer 24' between the n+ layer 23 of Photodiode PD, and n mold field 20, and is trying to miss the generating charge of Photodiode PD to n mold field 20 by impressing high + electrical potential difference to the LOD electrode 21. Although the potential barrier of p+ layer 24' exists also between Photodiode PD and the perpendicular transfer CCD, the charge which lowered the potential barrier of p+ layer 24', and was generated in Photodiode PD can be brought together in the bottom of the perpendicular transfer electrode a by impressing predetermined + electrical potential difference to the 1st perpendicular transfer electrode a. When high + electrical potential difference is impressed to the LOD electrode 21, although the charge generated with Photodiode PD flows to the perpendicular transfer CCD, since a few will mainly be thrown away into the direction of n mold field 20 for it by it, the sensibility (photoelectric conversion efficiency) of Photodiode PD falls substantially. Let this photoelectron abandonment period be a synchronous integral idle period (non-detecting phase). Moreover, when the applied voltage of the LOD electrode 21 is reduced and abandonment of a photoelectron is stopped, the charge generated with Photodiode PD will flow efficiently to the perpendicular transfer CCD, and will be accumulated in the bottom of a perpendicular transfer electrode. Let this photoelectron are recording period be a synchronous integral period (detection phase).

[0035]

Actuation of each period of are recording of the photoelectron by LOD mold IT-CCD, abandonment, and read-out is shown and explained to drawing 15 . In the are recording period of a photoelectron, the applied voltage of the LOD electrode 21 is low, and the sufficiently high electrical potential difference V1 is given to the perpendicular transfer electrode a currently formed next to Photodiode PD, and as shown in drawing 15 (a), the potential barrier by p+ layer 24' under a perpendicular transfer electrode currently formed between 25 and the n+ layer 23 n layers while lowering n layers of potentials of 25 is broken down. This is equivalent to electric switch S of drawing 1 (c) having closed. In this case, the photoelectron generated in the n+ layer 23 is accumulated in n layer 25 under a perpendicular transfer electrode.

[0036]

In the abandonment period of a photoelectron, the high + electrical potential difference Vs is impressed to the LOD electrode 21 connected to n mold field 20, and the potential of n mold

field 20 is lowered. When applied voltage Vs is sufficiently high, as shown in drawing 15 (b), the potential barrier by p+ layer 24' formed between n mold field 20 and the n+ layer 23 collapses, and many of photoelectrons generated in the n+ layer 23 are discarded by n mold field 20. At this time, an electrical potential difference V1 is kept impressed to the perpendicular transfer electrode a like the are recording period of a photoelectron. This is equivalent to what electric switch S of drawing 1 (c) has closed. If the applied voltage Vs of the LOD electrode 21 is set up so that the potential of n mold field 20 may become low rather than the potential of 25 n layers, since the photoelectron under a perpendicular transfer electrode generated in the n+ layer 23 can be drawn near to the one where potential is lower, most is discarded through n mold field 20 to the LOD electrode 21, without going to the perpendicular transfer electrode a side. Moreover, since the photoelectron under a perpendicular transfer electrode accumulated in 25 n layers has the potential barrier of the n+ layer 23 during the are recording period of a photoelectron, it is not discarded at the LOD electrode 21 (n mold field 20) side.

[0037]

Alternation of the are recording period (drawing 15 (a)) of a photoelectron and the abandonment period (drawing 15 (b)) of a photoelectron is carried out within a round term of exposure light, for example, they accumulate a photoelectron only with a specific detection phase (synchronous integral period) like drawing 2 (b), and discard a photoelectron in the remaining non-detecting phase (integral idle period). By repeating this actuation covering two or more periods of exposure light, the detection value equivalent to A0 of drawing 4 is acquired for every pixel. This detection value is read for a while.

[0038]

In the read-out period of the accumulated photoelectron, as shown in drawing 15 (c), the electrical potential difference V1 of the perpendicular transfer electrode a is set up low, the transfer clock of four phases is given to the transfer electrical potential differences V1-V4, and the accumulated signal charge is read so that n layers of potential barriers by p+ layer 24' of the perpendicular transfer CCD may be generated between 25 and the n+ layer 23 of Photodiode PD. This is equivalent to the condition that electric switch S of drawing 1 (b) opened.

[0039]

Thus, if the detection value equivalent to A0 of drawing 4 is acquired for every pixel next, the detection value equivalent to A1 of drawing 4 will be acquired for every pixel by shifting a detection phase 90 degrees and repeating are recording and abandonment of a photoelectron like drawing 2 (c), covering two or more periods of exposure light. If this detection value is read, the detection value equivalent to A2 of drawing 4 and A3 will be shortly acquired for every pixel drawing 2 (d) and by shifting a detection phase like 180 degrees and 270 degrees, going, and repeating are recording and abandonment of a photoelectron still like drawing 2 (e), covering two or more periods of exposure light. In addition, the count of the synchronous integral of each time does not have making it the same also until it says it.

[0040]

by the way, in IT-CCD which has a horizontal-type overflow drain electrode, since p mold substrate 22 can carry out until formation of the n+ field 23 which forms Photodiode PD deeply, there is an advantage which can raise the detection sensitivity to a near infrared ray. The area which forms the hemihedry and n mold field 20 which adjoined Photodiode PD and was connected to the LOD electrode 21 is required, and since the part and the light-receiving area of Photodiode PD become narrow, there is a fault in which a numerical aperture decreases. Moreover, in IT-CCD, since it is necessary to adjoin Photodiode PD and to form the perpendicular transfer CCD, the part and the light-receiving area of Photodiode PD are restricted. Then, FT-CCD which gave the transfer facility to photodiode PD itself and made light-receiving area large is explained below.

[0041]

(Gestalt 3 of operation)

Drawing 16 shows the configuration of frame transfer-die CCD (FT-CCD) which has a vertical mold overflow drain (VOD) electrode. It is formed in the front face of n mold substrate 30 so that the vertical mold overflow drain (VOD) electrode 31 which consists of an aluminum electrode

may contact a substrate directly without an insulator layer. Control voltage Vs is impressed to the VOD electrode 31. p mold field 32 is formed in the part surrounded with the VOD electrode 31 of the front face of n mold substrate 30. Long n mold field 35 is formed in two or more perpendicular directions in this p mold field 32. The part surrounded with the broken line of drawing 16 constitutes the photodiode PD for 1 pixel, and shows the cross-section structure to drawing 17 .

[0042]

In the front face of n mold field 35, it is SiO2. Along with the longitudinal direction of n mold field 35, two or more polish recon gate electrodes a, b, and c are formed through the becoming insulating thin film 36. With the longitudinal direction of n mold field 35, each polish recon gate electrodes a, b, and c are formed so that it may be extended perpendicularly, and they constitute one pixel from three gate electrodes a, b, and c. Although only the pixel of the limited number is illustrated in drawing 16 , they are horizontal and the thing which the pixel of the number according to vertical resolution consists of in fact.

[0043]

Polish recon gate electrodes a, b, c, and SiO2 Since the becoming insulating thin film 36 penetrates light, a photoelectron is generated in n mold field 35. However, parts other than the image pick-up section of drawing 16 are covered by the light-shielding film, and a photoelectron is generated neither in the are recording section nor the level transfer section. During a vertical-retrace-line period, the are recording section bundles up the signal charge of the image pick-up section, is transmitted at high speed, and reads the signal charge accumulated in the are recording section through the level transfer section to before a next vertical-retrace-line period. As it dissociates and the electrical potential differences phi1-phi3 impressed to the gate electrode of the are recording section have read the picture signal from the are recording section through the level transfer section, in the image pick-up section, its are recording of a signal charge is possible for the electrical potential differences V1-V6 impressed to the gate electrode of the image pick-up section. Therefore, if frame transfer-die CCD is used, it will become possible to take the long storage time of a synchronous integral compared with the case where INTARAIN transfer-die CCD is used. In this example, the transfer of a signal charge is enabled from the image pick-up section at the are recording section using the transfer electrical potential difference of six phases of V1-V6. On the other hand, the transfer of a signal charge is enabled at the level transfer section using the transfer electrical potential difference of the three phase circuit of phi1-phi3 from the are recording section. (Each gate electrode of the image pick-up section and the are recording section is connected through the same transfer electrical potential differences V1-V6 as the electrode horizontally located in a line, and wiring which is not illustrated so that phi1-phi3 may be impressed.) Although detailed explanation is omitted since the level transfer section is the same as the level transfer CCD mentioned above The transfer of a signal charge is enabled also here using the transfer electrical potential difference of two phases of VH1 and VH2.

[0044]

Drawing 18 shows electronic potential along with the broken line of drawing 17 . Between n mold field 35 which a photoelectron generates, and n mold substrate 30, as the broken line of drawing 18 shows, the potential barrier by p mold field 32 exists, but if high + electrical potential difference is impressed to the VOD electrode 31 connected to n mold substrate 30, this potential barrier can be broken down and a signal charge (photoelectron) can be thrown away into n mold substrate 30 from n mold field 35.

[0045]

Applied voltage Vs of the VOD electrode 31 is made low, and it is made for the potential barrier by p mold field 32 to exist between n mold field 35 and n mold substrate 30 in the are recording period of a photoelectron. Moreover, like drawing 19 (b), the gate electrodes a, b, and c of three per pixel are used, and not only the photoelectron generated under the gate electrode b by impressing highest + electrical potential difference to the central gate electrode b but the photoelectron generated under the gate electrodes a and c is accumulated in the potential well under the gate electrode b. This situation is shown in drawing 19 (Ha). Drawing 19 (Ha) shows

the potential of the electron about the thick alternate long and short dash line of drawing 19 (b). Moreover, drawing 19 (d) shows the potential of the electron about the thick broken line of drawing 19 (b) about each gate electrodes a, b, and c.
[0046]
In the abandonment period of a photoelectron, high + electrical potential difference is impressed to the VOD electrode 31, and as shown in drawing 19 (d), the height of the potential barrier by n mold field 35 and p mold field 32 between n mold substrates 30 is lowered, as shown in a continuous line from a broken line. At this time, the electrical potential difference impressed to the VOD electrode 31 is set up so that the potential of n mold substrate 30 may become lower than the potential of n mold field 35 under the gate electrodes a and c more highly than the potential of n mold field 35 under the gate electrode b. Although the electrical potential difference impressed to the gate electrodes a, b, and c is the same as that of the are recording period of a photoelectron, and the potential barrier by p mold field 32 is completely broken down under the gate electrodes a and c of both sides since + electrical potential difference higher than the gate electrodes a and c of both sides is impressed to the central gate electrode b Under the central gate electrode b, the potential barrier by p mold field 32 is not completely broken down only by height becoming low. For this reason, although many of photoelectrons generated under the gate electrodes a and c of both sides are discarded by n mold substrate 30, the photoelectron generated under the central gate electrode b is not discarded, and the photoelectron accumulated in the bottom of the central gate electrode b in the are recording period of a photoelectron is not discarded, either.
[0047]
When are recording and abandonment of an above-mentioned photoelectron are repeated two or more times, in the bottom of the central gate electrode b, the photoelectron accumulated in the central gate electrode b from the gate electrodes a and b of both sides in the are recording period of a photoelectron will be accumulated too much. Since the central gate electrode b is always accumulating the photoelectron, the average by the integral will always [this] be added to the detection value by the synchronous integral, but since the detection value by the synchronous integral has still been acquired from the gate electrodes a and b of both sides, sufficient contrast can be acquired.
[0048]
Moreover, like this example, since distance information is computable also by observing two or more sheets, shifting the phase of the are recording period of a photoelectron [as opposed to exposure light for the image which made one half the are recording period of a photoelectron, for example among round terms of exposure light, and carried out the synchronous integral of the remaining one half as an abandonment period of a photoelectron], since contrast becomes high, FT-CCD can be used for an application with the long are recording period of a photoelectron.
[0049]
furthermore, it was called not only the gate electrode of three sheets but five sheets and seven sheets -- many -- if 1 pixel is constituted from a gate electrode of several sheets and it is made to centralize a photoelectron on the central gate electrode of one sheet, rather than the component of the average by the integral, the component of the detection value by the synchronous integral collected from the surrounding gate electrode becomes large relatively, and can always in a central gate electrode improve contrast further.
[0050]
In addition, since the vertical mold overflow drain electrode 31 needs to form an aluminum electrode so that p mold field 32 may be surrounded in n mold substrate 30 around p mold field 32, p mold field 32 cannot be formed with epitaxial growth. when it forms by the diffusion method, the until formation of the p mold field cannot be carried out not much deeply. Therefore, n mold field 35 used as a photodiode will be formed still more shallowly than p mold field 32, and its sensibility to a near infrared ray is low. in order to cancel this fault, FT-CCD which has the horizontal-type overflow drain (LOD) electrode which can carry out until formation of the n+ field of Photodiode PD deeply is explained below.
[0051]

(Gestalt 4 of operation)
Drawing 20 shows the configuration of frame transfer-die CCD (FT-CCD) which has a horizontal-type overflow drain (LOD) electrode. The part surrounded with the broken line of drawing 20 constitutes the photodiode PD for 1 pixel, and shows the cross-section structure to drawing 21 . p mold field 42' is formed in the front face of p mold substrate 42 of epitaxial growth so that n mold field 45 used as a photodiode can be formed deeply. By the ability forming deeply n mold field 45 used as a photodiode, there is the description which can make sensibility to a near infrared high. n mold field 45 used as a photodiode is adjoined, the p+ field 44 is formed, and n mold field 40 used as a horizontal-type overflow drain is formed in this p+ field 44. n mold field 40 used as n mold field 45 used as a photodiode and a horizontal-type overflow drain has extended for a long time in the perpendicular direction of transfer of a substrate adjacently, and the n mold each field 40 is connected to the horizontal-type overflow drain (LOD) electrode 41 which consists of an aluminum electrode. Control voltage Vs is impressed to the LOD electrode 41.

[0052]
In the front face of n mold field 45, it is SiO2. Along with the longitudinal direction of n mold field 45, two or more polish recon gate electrodes a, b, and c are formed through the becoming insulating thin film 46. With the longitudinal direction of n mold field 45, each polish recon gate electrodes a, b, and c are formed so that it may be extended perpendicularly, and they constitute one pixel from three gate electrodes a, b, and c. Although only the pixel of the limited number is illustrated in drawing 20 , they are horizontal and the thing which the pixel of the number according to vertical resolution consists of in fact.

[0053]
Polish recon gate electrodes a, b, c, and SiO2 Since the becoming insulating thin film 46 penetrates light, a photoelectron is generated in n mold field 45. However, parts other than the image pick-up section of drawing 20 are covered by the light-shielding film, and a photoelectron is generated neither in the are recording section nor the level transfer section. During a vertical-retrace-line period, the are recording section bundles up the signal charge of the image pick-up section, is transmitted at high speed, and reads the signal charge accumulated in the are recording section through the level transfer section to before a next vertical-retrace-line period. As it dissociates and the electrical potential differences phi1-phi3 impressed to the gate electrode of the are recording section have read the picture signal from the are recording section through the level transfer section, in the image pick-up section, its are recording of a signal charge is possible for the electrical potential differences V1-V6 impressed to the gate electrode of the image pick-up section. Therefore, if frame transfer-die CCD is used, it will become possible to take the long storage time of a synchronous integral compared with the case where INTARAIN transfer-die CCD is used. In this example, the transfer of a signal charge is enabled from the image pick-up section at the are recording section using the transfer electrical potential difference of six phases of V1-V6. On the other hand, the transfer of a signal charge is enabled at the level transfer section using the transfer electrical potential difference of the three phase circuit of phi1-phi3 from the are recording section. (Each gate electrode of the image pick-up section and the are recording section is connected through the same transfer electrical potential differences V1-V6 as the electrode horizontally located in a line, and wiring which is not illustrated so that phi1-phi3 may be impressed.) Although detailed explanation is omitted since the level transfer section is the same as the level transfer CCD mentioned above The transfer of a signal charge is enabled also here using the transfer electrical potential difference of two phases of VH1 and VH2.

[0054]
Drawing 22 shows electronic potential along with the broken line of drawing 21 . Although the potential barrier by the p+ field 44 exists between n mold fields 40 which adjoin n mold field 45 which a photoelectron generates, and this through the p+ field 44 as the broken line of drawing 22 shows If high + electrical potential difference is impressed to the LOD electrode 41 connected to n mold field 40, this potential barrier can be broken down and a signal charge (photoelectron) can be thrown away into the LOD electrode 41 through n mold field 40 from n

mold field 45.
[0055]
Applied voltage Vs of the LOD electrode 41 is made low, and it is made for the potential barrier by the p+ field 44 to exist between n mold field 45 and n mold field 40 in the are recording period of a photoelectron. Moreover, like drawing 23 (b), the gate electrodes a, b, and c of three per pixel are used, and not only the photoelectron generated under the gate electrode b by impressing highest + electrical potential difference to the central gate electrode b but the photoelectron generated under the gate electrodes a and c is accumulated in the potential well under the gate electrode b. This situation is shown in drawing 23 (Ha). Drawing 23 (Ha) shows the potential of the electron about the thick alternate long and short dash line of drawing 23 (b). Moreover, drawing 23 (d) shows the potential of the electron about the thick broken line of drawing 23 (b) about each gate electrodes a, b, and c.
[0056]
In the abandonment period of a photoelectron, high + electrical potential difference is impressed to the LOD electrode 41, and as shown in drawing 23 (d), the height of the potential barrier by the p+ field 44 between n mold field 45 and n mold field 40 is lowered. At this time, the electrical potential difference Vs impressed to the LOD electrode 41 is set up so that the potential of n mold field 40 may become lower than the potential of n mold field 45 under the gate electrodes a and c more highly than the potential of n mold field 45 under the gate electrode b. Although the electrical potential difference impressed to the gate electrodes a, b, and c is the same as that of the are recording period of a photoelectron, and the potential barrier by the p+ field 44 is completely broken down under the gate electrodes a and c of both sides since + electrical potential difference higher than the gate electrodes a and c of both sides is impressed to the central gate electrode b Under the central gate electrode b, the potential barrier by the p+ field 44 is not completely broken down only by height becoming low. For this reason, although many of photoelectrons generated under the gate electrodes a and c of both sides are discarded by n mold field 40, the photoelectron generated under the central gate electrode b is not discarded, and the photoelectron accumulated in the bottom of the central gate electrode b in the are recording period of a photoelectron is not discarded, either.
[0057]
When are recording and abandonment of an above-mentioned photoelectron are repeated two or more times, in the bottom of the central gate electrode b, the photoelectron accumulated in the central gate electrode b from the gate electrodes a and b of both sides in the are recording period of a photoelectron will be accumulated too much. Since the central gate electrode b is always accumulating the photoelectron, the average by the integral will always [this] be added to the detection value by the synchronous integral, but since the detection value by the synchronous integral has still been acquired from the gate electrodes a and b of both sides, sufficient contrast can be acquired.
[0058]
Although the gestalten 3 and 4 of operation shown in drawing 16 - drawing 23 explained the case where 1 pixel was constituted from a gate electrode of three sheets, as shown in drawing 24 or drawing 25 , when it constitutes 1 pixel from a gate electrode of four or more sheets, it is good to form a potential barrier so that a photoelectron may not flow into the gate electrode which is accumulating the photoelectron in the period which discards a charge from a perimeter. When drawing 24 constitutes 1 pixel from a gate electrode of four sheets, drawing 25 is the case where 1 pixel is constituted from a gate electrode of six sheets, and shows the potential of the electron under each gate electrode [in / (a) a charge storage period and / in (b) / a charge abandonment period]. The part shown in gray in drawing 24 and drawing 25 is a photoelectron. In the charge storage period of (a) The photoelectron generated under the surrounding gate electrode is flowed and accumulated in the bottom of a gate electrode with the electronic lowest potential. In the charge abandonment period of (b) It is controlling to form a potential barrier in the bottom of an adjoining gate electrode to isolate electrically the part in which the photoelectron under a gate electrode with the electronic lowest potential was accumulated from a perimeter.
[0059]

If the potential of the electron under each gate electrode in a charge storage period and a charge abandonment period is shown in three dimension about the case where 1 pixel is constituted from a gate electrode of six sheets shown in drawing 25 , it will become as shown in drawing 27 (a) and (b). V1-V6 in drawing support the perpendicular transfer electrical potential difference shown in drawing 20 , and LOD supports n mold field 40 used as a horizontal-type overflow drain. While the photoelectron under the gate electrode to which the electrical potential difference of V2 and V6 was impressed moves in the charge storage period of drawing 27 (a) to the bottom of the gate electrode to which the electrical potential difference of V3 and V5 was impressed The photoelectron under the gate electrode to which the electrical potential difference of V3 and V5 was impressed moves to the bottom of the gate electrode to which the electrical potential difference of V4 was impressed, and a photoelectron is accumulated in the bottom of the gate electrode to which this electrical potential difference of V4 was impressed. the charge abandonment period of drawing 27 (b) -- the electrical potential difference of V3 and V5 -- V1 and until comparable -- the part in which the photoelectron under the gate electrode to which the electrical potential difference of V4 was impressed was accumulated by making it low is electrically isolated from a perimeter, and the inflow of a photoelectron is prevented. Moreover, by setting up lower [it is higher than the gate electrode to which the electrical potential difference of V4 was impressed for the potential of the electron of a LOD electrode, and] than the gate electrode to which the electrical potential difference of V2 and V6 was impressed The photoelectron generated under the gate electrode to which the electrical potential difference of V2 and V6 was impressed is discarded by the LOD electrode, without discarding the photoelectron accumulated in the bottom of the gate electrode to which the electrical potential difference of V4 was impressed.

[0060]

By the way, some photoelectrons of a non-detecting phase flow into the polar zone for are recording (electrode of the location where electronic potential is the deepest) to which the electrical potential difference of V4 was impressed in the example of drawing 25 . Moreover, the polar zone for are recording itself generates and accumulates the photoelectron of a non-detecting phase. The photoelectron of the phase non-detecting [these] serves as DC component to the photoelectron of a detection phase, and reduces a S/N ratio. Then, if a light-shielding film 47 is formed in the front face of the sensitization section for charge storages, and the sensitization section which forms a potential barrier as shown in drawing 26 , the ratio of an integral can always to a synchronous integral be reduced, and the contrast of a synchronous integral can be improved. In the example of drawing 26 , the front face of the gate electrode to which the electrical potential difference of V1, V3, V4, and V5 is impressed is covered by the light-shielding film 47 so that a photoelectron may be generated only under the gate electrode to which the electrical potential difference of V2 and V6 is impressed.

[0061]

In addition, this invention is applicable similarly not only by IT-CCD or FT-CCD but FIT-CCD (frame INTARAIN transfer-die CCD) which is these compound dies. Although the are recording section for one screen is added between the level transfer section of IT-CCD, and the image pick-up section as shown in drawing 28 , as for FIT-CCD, two kinds of perpendicular transfer electrical potential differences are needed and actuation becomes complicated, there is an advantage which can reduce the smear which is the fault of IT-CCD.

[0062]

[Effect of the Invention]

Since sensibility of the sensitization section was made adjustable synchronizing with the exposure light by which intensity modulation was carried out according to invention of claim 1, electro-optical distance measurement is realizable with an easy configuration.

Since sensibility of the sensitization section was made adjustable synchronizing with the exposure light by which intensity modulation was carried out according to invention of claim 2, the electric switch which can open and close migration of the signal charge from the sensitization section to the are recording section by high frequency is unnecessary, and there is an available advantage also with the image sensor of applications other than a synchronous

integral.
Since the same actuation as a synchronous integral was made realizable using the INTARAIN transfer-die CCD image sensor which has the most common vertical mold overflow drain electrode as a CCD image sensor according to invention of claim 3, electro-optical distance measurement can be realized cheaply, without using a special image sensor.
[0063]
Since the same actuation as a synchronous integral was made realizable using the CCD image sensor which has a horizontal-type overflow drain electrode with high sensibility to a near infrared according to invention of claims 4 or 6, ranging with the high night vision engine performance becomes possible.
According to invention of claims 5 or 6, since frame transfer-die CCD is used, it becomes possible to take the long storage time of a synchronous integral compared with the case where INTARAIN transfer-die CCD is used.
[0064]
According to invention of claim 7, in a charge abandonment period, since the potential barrier which isolates the sensitization section for charge storages electrically from other sensitization sections was formed, the contrast of a synchronous integral is improvable.
Since the protection-from-light section was prepared in the front face of the sensitization section for charge storages, and the sensitization section which forms a potential barrier according to invention of claim 8, the ratio of an integral can always to a synchronous integral be reduced, and the contrast of a synchronous integral can be improved.
Since the electric switch which can open and close migration of the signal charge from the sensitization section to the are recording section by high frequency is formed for every sensor element according to invention of claim 9 and only the signal charge of a detection phase can be accumulated alternatively, the contrast of a synchronous integral is improvable.
Since the transfer electrode prepared in order to make the are recording section serve a double purpose as the transfer section was further made to serve a double purpose as an electric switch for opening and closing migration of the signal charge from the sensitization section to the are recording section by high frequency according to invention of claim 10, actuation of a synchronous integral is realizable with an easy configuration.
[Brief Description of the Drawings]
[Drawing 1] It is the explanatory view showing the basic configuration of this invention, and the block diagram in which (a) shows a whole configuration, the important section block diagram in which (b) shows an example of an image sensor, and (c) are the important section block diagrams showing other examples of an image sensor.
[Drawing 2] It is the explanatory view of operation showing the timing of the synchronous integral by the image sensor of this invention.
[Drawing 3] It is the outline block diagram of optical system used for the conventional electro-optical distance measurement.
[Drawing 4] It is the principle explanatory view of the conventional electro-optical distance measurement.
[Drawing 5] It is the important section block diagram showing an example of the image sensor used for the conventional electro-optical distance measurement.
[Drawing 6] It is the important section block diagram showing other examples of the image sensor used for the conventional electro-optical distance measurement.
[Drawing 7] It is the top view showing the whole image sensor configuration of the gestalt 1 of operation of this invention.
[Drawing 8] It is the perspective view showing the important section configuration of the image sensor of the gestalt 1 of operation of this invention.
[Drawing 9] It is the sectional view showing the important section configuration of the image sensor of the gestalt 1 of operation of this invention.
[Drawing 10] It is the explanatory view showing the potential of the electron of the image sensor of the gestalt 1 of operation of this invention.
[Drawing 11] It is the explanatory view of the image sensor of the gestalt 1 of operation of this

invention of operation.
[Drawing 12] It is the top view showing the whole image sensor configuration of the gestalt 2 of operation of this invention.
[Drawing 13] It is the perspective view showing the important section configuration of the image sensor of the gestalt 2 of operation of this invention.
[Drawing 14] It is the explanatory view showing the potential of the electron of the image sensor of the gestalt 2 of operation of this invention.
[Drawing 15] It is the explanatory view of the image sensor of the gestalt 2 of operation of this invention of operation.
[Drawing 16] It is the top view showing the whole image sensor configuration of the gestalt 3 of operation of this invention.
[Drawing 17] It is the perspective view showing the important section configuration of the image sensor of the gestalt 3 of operation of this invention.
[Drawing 18] It is the explanatory view showing the potential of the electron of the image sensor of the gestalt 3 of operation of this invention.
[Drawing 19] It is the explanatory view of the image sensor of the gestalt 3 of operation of this invention of operation.
[Drawing 20] It is the top view showing the whole image sensor configuration of the gestalt 4 of operation of this invention.
[Drawing 21] It is the perspective view showing the important section configuration of the image sensor of the gestalt 4 of operation of this invention.
[Drawing 22] It is the explanatory view showing the potential of the electron of the image sensor of the gestalt 4 of operation of this invention.
[Drawing 23] It is the explanatory view of the image sensor of the gestalt 4 of operation of this invention of operation.
[Drawing 24] It is the explanatory view showing actuation of FT-CCD using the gate voltage of four phases.
[Drawing 25] It is the explanatory view showing actuation of FT-CCD using the gate voltage of six phases.
[Drawing 26] It is the explanatory view showing the actuation at the time of adding a light-shielding film to the sensitization section of FT-CCD using the gate voltage of six phases.
[Drawing 27] It is the explanatory view showing actuation of FT-CCD using the gate voltage of six phases in three dimension.
[Drawing 28] It is the top view showing a whole FIT-CCD configuration.
[Description of Notations]
1 Light Source
2 Detected Material
3 Image Formation Optical System
4 Image Sensor
5 Sensibility Control Section
6 Storage Section
7 Detection Phase Setting Section
8 Ranging Operation Part

[Translation done.]

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the explanatory view showing the basic configuration of this invention, and the block diagram in which (a) shows a whole configuration, the important section block diagram in which (b) shows an example of an image sensor, and (c) are the important section block diagrams showing other examples of an image sensor.
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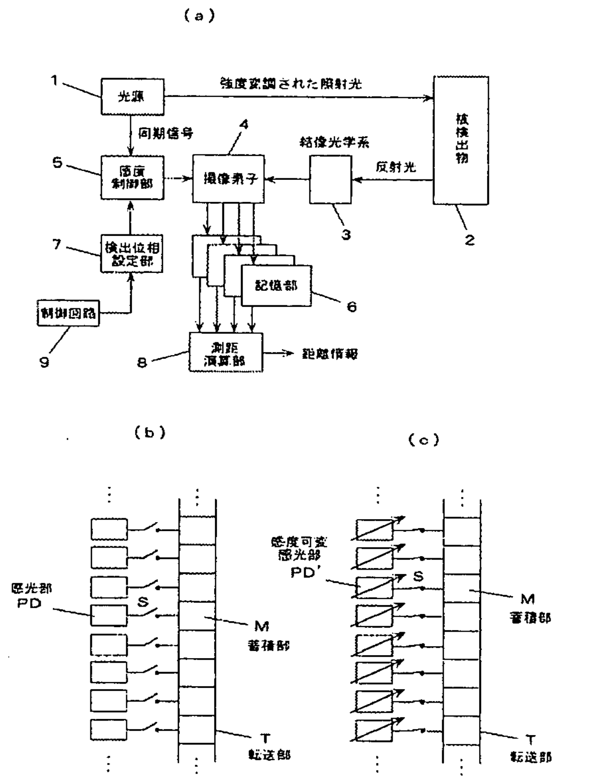
[Drawing 15] It is the explanatory view of the image sensor of the gestalt 2 of operation of this invention of operation.
[Drawing 16] It is the top view showing the whole image sensor configuration of the gestalt 3 of operation of this invention.
[Drawing 17] It is the perspective view showing the important section configuration of the image sensor of the gestalt 3 of operation of this invention.
[Drawing 18] It is the explanatory view showing the potential of the electron of the image sensor of the gestalt 3 of operation of this invention.
[Drawing 19] It is the explanatory view of the image sensor of the gestalt 3 of operation of this invention of operation.
[Drawing 20] It is the top view showing the whole image sensor configuration of the gestalt 4 of operation of this invention.
[Drawing 21] It is the perspective view showing the important section configuration of the image sensor of the gestalt 4 of operation of this invention.
[Drawing 22] It is the explanatory view showing the potential of the electron of the image sensor of the gestalt 4 of operation of this invention.
[Drawing 23] It is the explanatory view of the image sensor of the gestalt 4 of operation of this

invention of operation.
[Drawing 24] It is the explanatory view showing actuation of FT-CCD using the gate voltage of four phases.
[Drawing 25] It is the explanatory view showing actuation of FT-CCD using the gate voltage of six phases.
[Drawing 26] It is the explanatory view showing the actuation at the time of adding a light-shielding film to the sensitization section of FT-CCD using the gate voltage of six phases.
[Drawing 27] It is the explanatory view showing actuation of FT-CCD using the gate voltage of six phases in three dimension.
[Drawing 28] It is the top view showing a whole FIT-CCD configuration.
[Description of Notations]
1 Light Source
2 Detected Material
3 Image Formation Optical System
4 Image Sensor
5 Sensibility Control Section
6 Storage Section
7 Detection Phase Setting Section
8 Ranging Operation Part

[Translation done.]

DRAWINGS

[Drawing 1]


(a)
1
光源
強度変調された照射光
被検出物
2
同期信号
4
結像光学系
5
感度制御部
撮像素子
反射光
3
7
検出位相設定部
記憶部
6
制御回路
9
8
測距演算部
距離情報
(b)
(c)
感光部
PD
S
M
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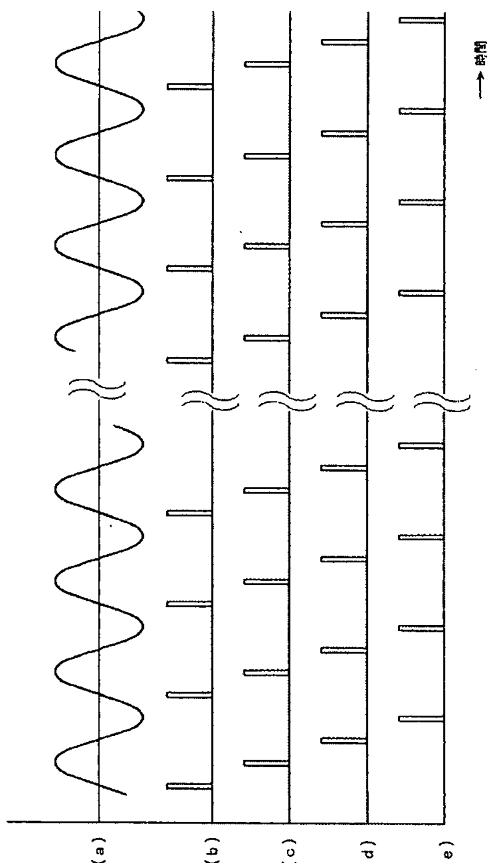
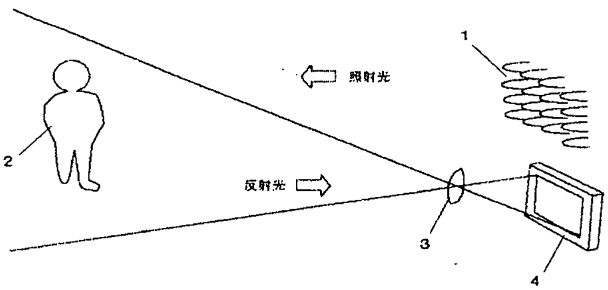
[Drawing 2]


時間
(a)
(b)
(c)
(d)
(e)

[Drawing 3]



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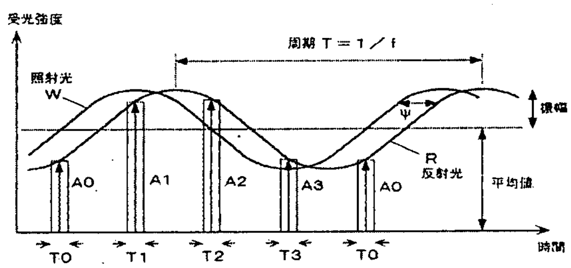

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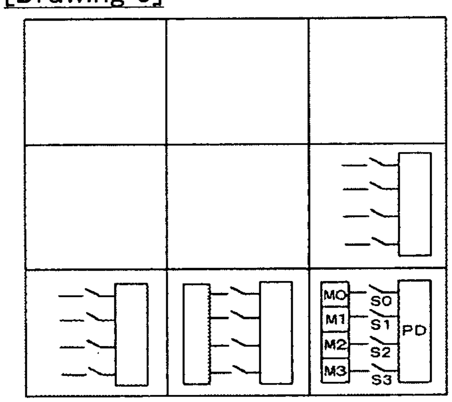

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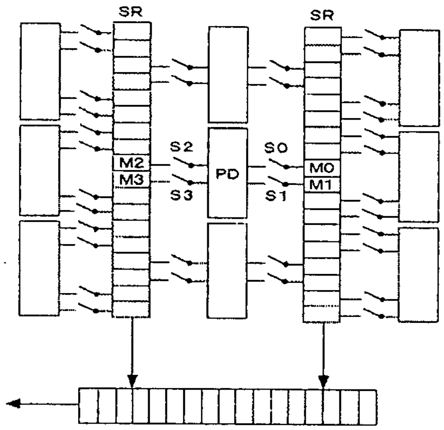

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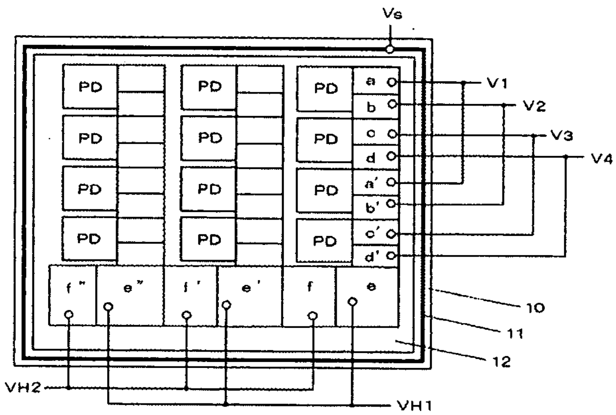

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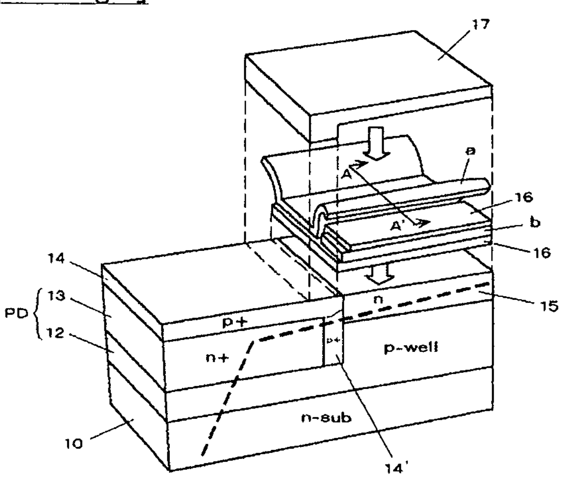

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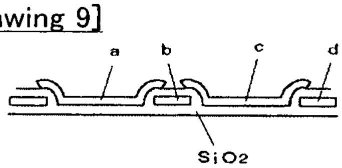
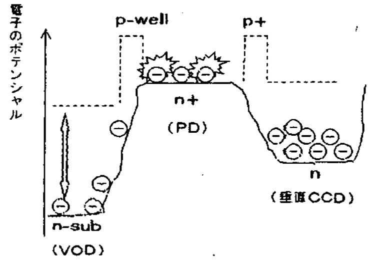


[Drawing 10]



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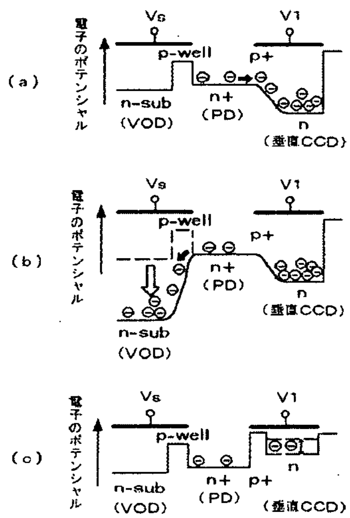

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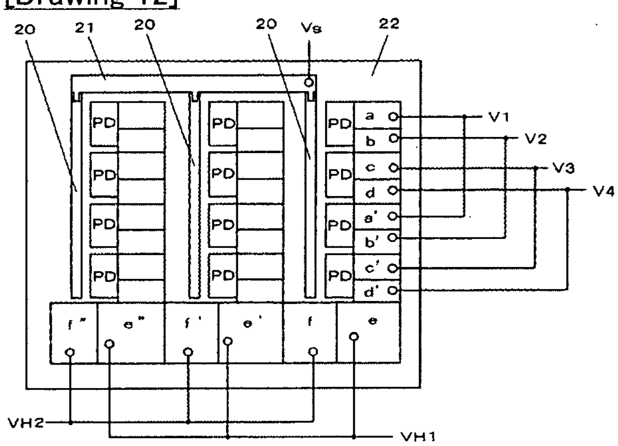

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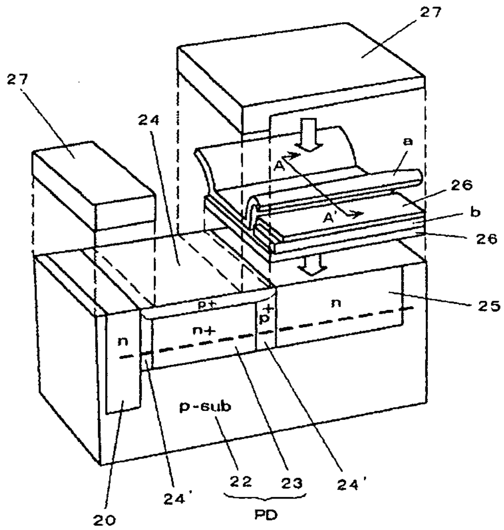

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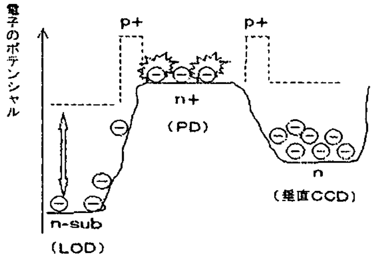

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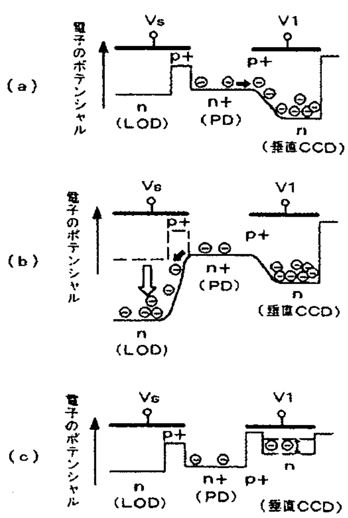

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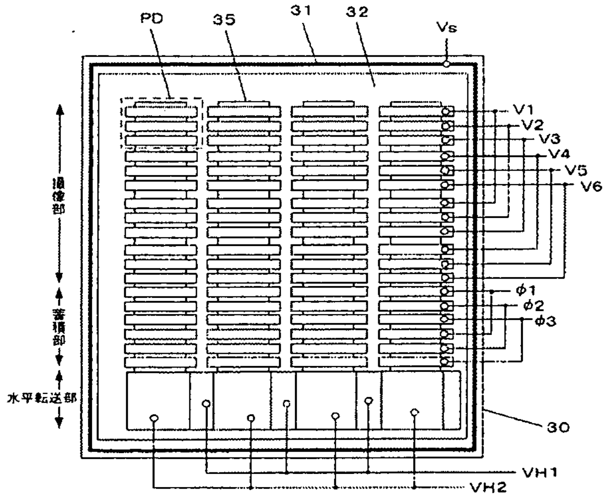

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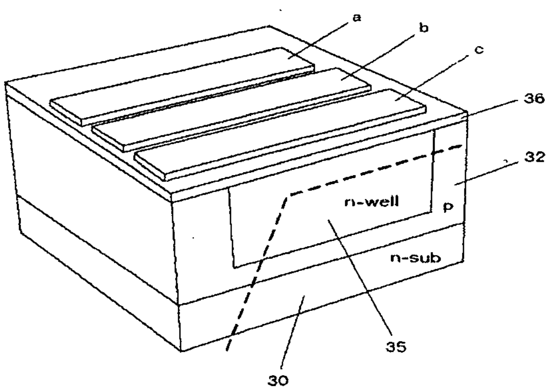

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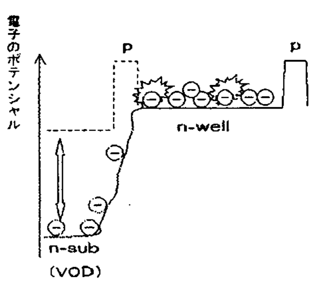

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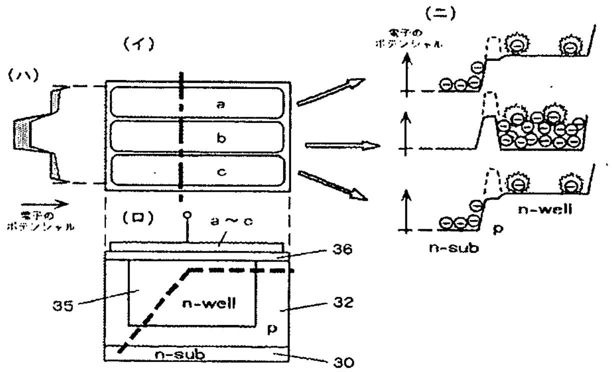

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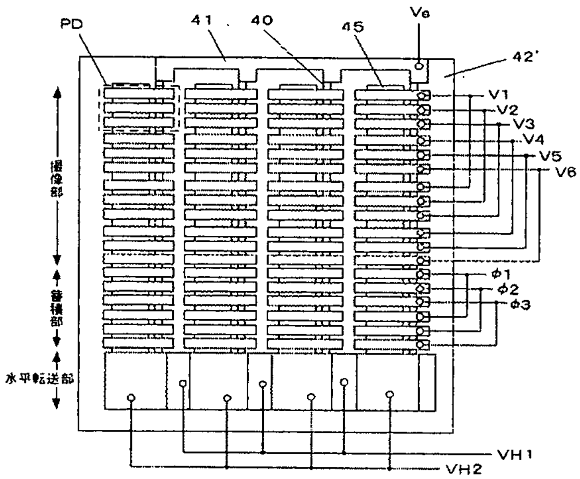

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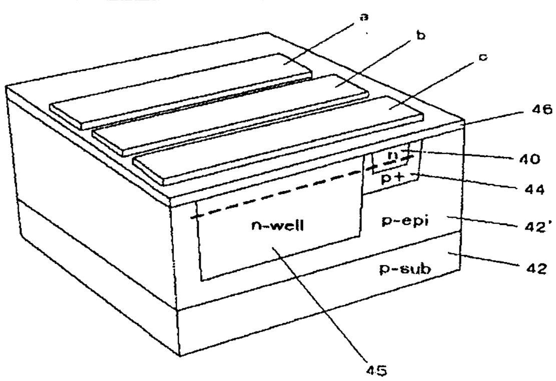

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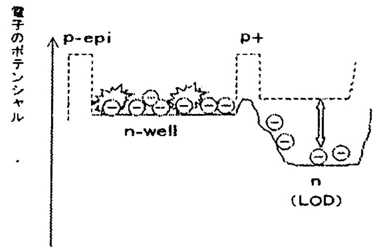
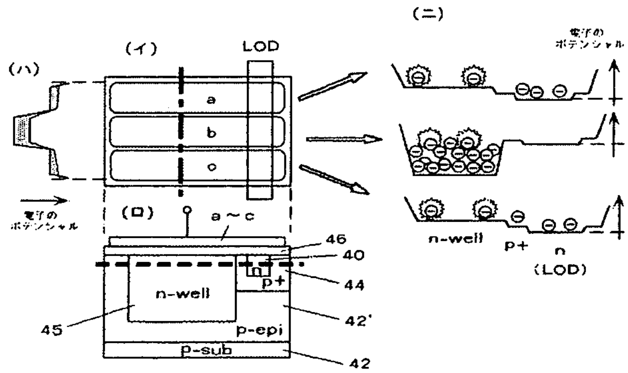


[Drawing 23]



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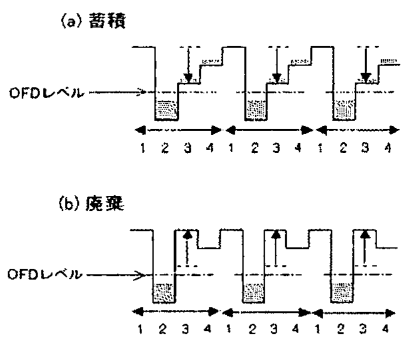

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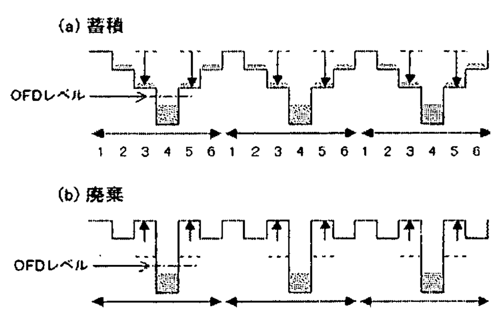
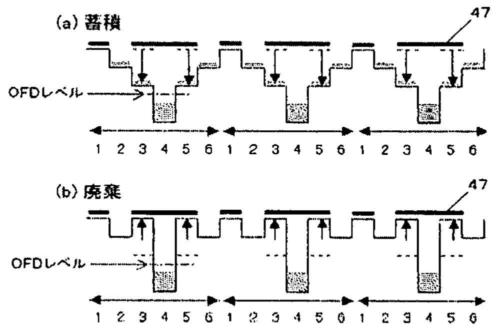


[Drawing 26]



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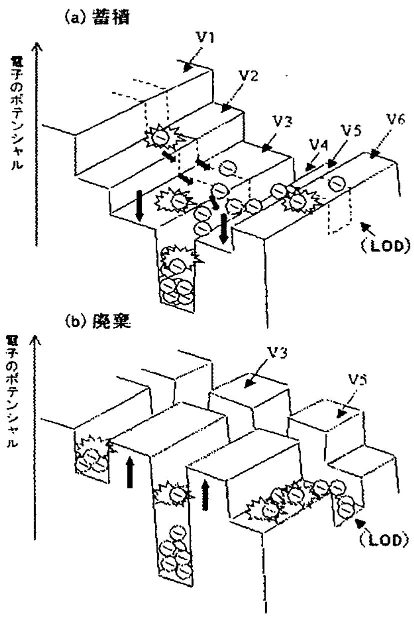
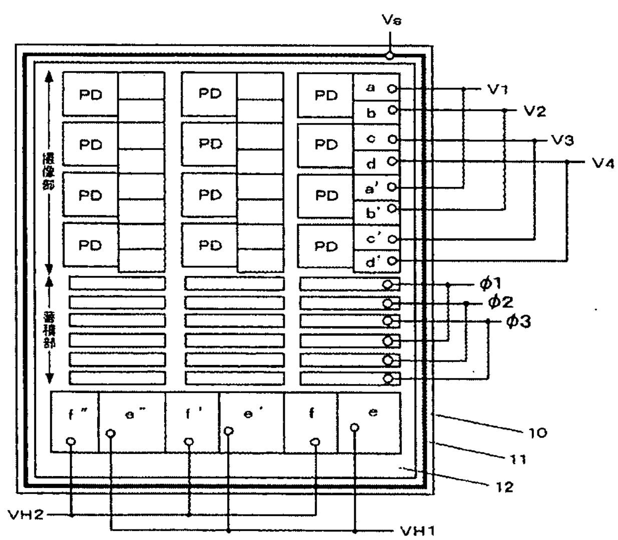


[Drawing 28]



[Translation done.]

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// H04N 5/335	H04N 5/335	P	

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最終頁に続く

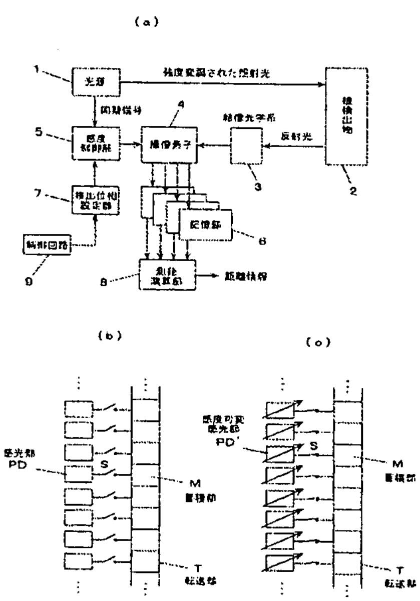
(54)【発明の名称】撮像素子を用いた測距装置および測距方法

(57)【要約】

【課題】一般的なＣＣＤ撮像素子の制御方法を工夫することで、実質的に同期積分をしているのと同じような動作を実現可能とし、従来、特殊な構造の撮像素子を必要としていた光波測距を一般的なＣＣＤ撮像素子を用いて安価に実現する。

【解決手段】複数の感光部を半導体基板上に１次元または２次元的に配列され、前記半導体基板への電圧印加により前記各感光部の感度を制御可能な構造を有する撮像素子４と、強度変調された光の変調信号に同期して前記撮像素子４の半導体基板に前記各感光部の感度を変調せしめる電圧を印加する感度制御部５とを有する構成とし、強度変調された照射光に同期して感光部の感度を可変とすることで光波測距を実現する。

【選択図】　図１



【特許請求の範囲】
【請求項１】
複数の感光部を半導体基板上に１次元または２次元的に配列され、前記半導体基板への電圧印加により前記各感光部の感度を制御可能な構造を有する撮像素子と、強度変調された光の変調信号に同期して前記撮像素子の半導体基板に前記各感光部の感度を変調せしめる電圧を印加する感度制御部とを有することを特徴とする撮像素子を用いた測距装置。
【請求項２】
受光量に応じて信号電荷を発生せしめる感光部と、感光部で発生した信号電荷を蓄積する蓄積部とを備えるセンサ要素を半導体基板上に１次元または２次元的に配列すると共に、各センサ要素の蓄積部から蓄積電荷を読み出す転送部を前記半導体基板に形成し、前記半導体基板への電圧印加により感光部の感度を実質的に低下させることができる構造を有する撮像素子と、
強度変調された光により照射された被検出物からの反射光を前記撮像素子のセンサ要素が配列された面に結像せしめる結像光学系と、
前記強度変調された光の変調信号に同期して、前記感光部の感度を低下させるための制御電圧を前記半導体基板に印加する感度制御部と、
前記強度変調の複数の周期にわたって前記撮像素子の蓄積部に蓄積された電荷を前記転送部により読み出して測定値として記憶する記憶部と、
前記強度変調の一周期のうち前記感光部の感度を低下させるための制御電圧が印加される低感度期間の位相を前記記憶部に測定値が記憶されるたびに切り替える検出位相設定部と、
記憶部に記憶された低感度期間の位相が異なる複数の測定値に基づいて、各センサ要素ごとに被検出物までの距離情報を演算する測距演算部とを有することを特徴とする撮像素子を用いた測距装置。
【請求項３】
受光量に応じて信号電荷を発生せしめる感光部と、感光部で発生した信号電荷を蓄積する蓄積部とを備えるセンサ要素を半導体基板上に２次元的に配列すると共に、各センサ要素の蓄積部から蓄積電荷を読み出す転送部を前記半導体基板に形成し、前記半導体基板の表面と垂直な方向に感光部の電位障壁を崩すような高い電圧を印加することにより感光部の信号電荷を前記半導体基板に廃棄するための縦型オーバーフロードレイン電極を有するインターライン・トランスファ型ＣＣＤ撮像素子を用いた測距方法であって、
強度変調された光により照射された被検出物からの反射光を前記撮像素子のセンサ要素が配列された面に結像せしめた状態で、前記強度変調された光の変調信号に同期して、前記強度変調の一周期のうち所定の期間で前記感光部の信号電荷を前記半導体基板に廃棄させるための制御電圧を前記縦型オーバーフロードレイン電極に印加する動作を前記強度変調の複数の周期にわたって繰り返す第１の段階と、
第１の段階で前記撮像素子の蓄積部に蓄積された電荷を測定値として前記転送部により読み出す第２の段階と、
第２の段階で測定値が読み出されるたびに、第１の段階で前記縦型オーバーフロードレイン電極に前記制御電圧を印加する期間の位相を切り替える第３の段階と、
第１、第２、第３の段階を複数回繰り返した後、前記制御電圧を印加する期間の位相が異なる複数の測定値に基づいて、各センサ要素ごとに被検出物までの距離情報を演算する第４の段階とを有することを特徴とする撮像素子を用いた測距方法。
【請求項４】
受光量に応じて信号電荷を発生せしめる感光部と、感光部で発生した信号電荷を蓄積する蓄積部とを備えるセンサ要素を半導体基板上に２次元的に配列すると共に、各センサ要素の蓄積部から蓄積電荷を読み出す転送部を前記半導体基板に形成し、前記半導体基板の表面と水平な方向に感光部の電位障壁を崩すような高い電圧を印加することにより感光部の信号電荷を前記半導体基板の表面と水平な方向に廃棄するための横型オーバーフロードレイン電極を有するインターライン・トランスファ型ＣＣＤ撮像素子を用いた測距方法であ

って、
強度変調された光により照射された被検出物からの反射光を前記撮像素子のセンサ要素が配列された面に結像せしめた状態で、前記強度変調された光の変調信号に同期して、前記強度変調の一周期のうち所定の期間で前記感光部の信号電荷を廃棄させるための制御電圧を前記横型オーバーフロードレイン電極に印加する動作を前記強度変調の複数の周期にわたって繰り返す第１の段階と、
第１の段階で前記撮像素子の蓄積部に蓄積された電荷を測定値として前記転送部により読み出す第２の段階と、
第２の段階で測定値が読み出されるたびに、第１の段階で前記横型オーバーフロードレイン電極に前記制御電圧を印加する期間の位相を切り替える第３の段階と、
第１、第２、第３の段階を複数回繰り返した後、前記制御電圧を印加する期間の位相が異なる複数の測定値に基づいて、各センサ要素ごとに被検出物までの距離情報を演算する第４の段階とを有することを特徴とする撮像素子を用いた測距方法。
【請求項５】
受光量に応じてそれぞれ信号電荷を発生せしめる３つ以上の感光部を備え、両端を除く特定の感光部に他の感光部から信号電荷を集めるような電位を与えることにより前記特定の感光部に信号電荷を蓄積するようにしたセンサ要素を半導体基板上に２次元的に配列して成る撮像部と、撮像部の各センサ要素から蓄積電荷を読み出す転送部を前記半導体基板に形成し、前記半導体基板の表面と垂直な方向に感光部の電位障壁を崩すような高い電圧を印加することにより感光部の信号電荷を前記半導体基板に廃棄するための縦型オーバーフロードレイン電極を有するフレーム・トランスファ型ＣＣＤ撮像素子を用いた測距方法であって、
強度変調された光により照射された被検出物からの反射光を前記撮像素子のセンサ要素が配列された面に結像せしめた状態で、前記強度変調された光の変調信号に同期して、前記強度変調の一周期のうち所定の期間で前記各センサ要素を構成する３つ以上の感光部のうち前記特定の感光部に蓄積された信号電荷を残したまま他の感光部の信号電荷を前記半導体基板に廃棄させるような制御電圧を前記縦型オーバーフロードレイン電極に印加する動作を前記強度変調の複数の周期にわたって繰り返す第１の段階と、
第１の段階で前記各センサ要素の前記特定の感光部に蓄積された電荷を測定値として前記転送部により読み出す第２の段階と、
第２の段階で測定値が読み出されるたびに、第１の段階で前記縦型オーバーフロードレイン電極に前記制御電圧を印加する期間の位相を切り替える第３の段階と、
第１、第２、第３の段階を複数回繰り返した後、前記制御電圧を印加する期間の位相が異なる複数の測定値に基づいて、各センサ要素ごとに被検出物までの距離情報を演算する第４の段階とを有することを特徴とする撮像素子を用いた測距方法。
【請求項６】
受光量に応じてそれぞれ信号電荷を発生せしめる３つ以上の感光部を備え、両端を除く特定の感光部に他の感光部から信号電荷を集めるような電位を与えることにより前記特定の感光部に信号電荷を蓄積するようにしたセンサ要素を半導体基板上に２次元的に配列して成る撮像部と、撮像部の各センサ要素から蓄積電荷を読み出す転送部を前記半導体基板に形成し、前記半導体基板の表面と水平な方向に感光部の電位障壁を崩すような高い電圧を印加することにより感光部の信号電荷を廃棄するための横型オーバーフロードレイン電極を有するフレーム・トランスファ型ＣＣＤ撮像素子を用いた測距方法であって、
強度変調された光により照射された被検出物からの反射光を前記撮像素子のセンサ要素が配列された面に結像せしめた状態で、前記強度変調された光の変調信号に同期して、前記強度変調の一周期のうち所定の期間で前記各センサ要素を構成する３つ以上の感光部のうち前記特定の感光部に蓄積された信号電荷を残したまま他の感光部の信号電荷を廃棄させるような制御電圧を前記横型オーバーフロードレイン電極に印加する動作を前記強度変調の複数の周期にわたって繰り返す第１の段階と、
第１の段階で前記各センサ要素の前記特定の感光部に蓄積された電荷を測定値として前記

転送部により読み出す第２の段階と、
第２の段階で測定値が読み出されるたびに、第１の段階で前記横型オーバーフロードレイン電極に前記制御電圧を印加する期間の位相を切り替える第３の段階と、
第１、第２、第３の段階を複数回繰り返した後、前記制御電圧を印加する期間の位相が異なる複数の測定値に基づいて、各センサ要素ごとに被検出物までの距離情報を演算する第４の段階とを有することを特徴とする撮像素子を用いた測距方法。
【請求項７】
請求項５または６において、前記各センサ要素を構成する感光部は４つ以上で構成されており、前記特定の感光部に蓄積された信号電荷を残したまま他の感光部の信号電荷を廃棄させる期間では、前記特定の感光部に隣接する感光部に前記特定の感光部を他の感光部から電気的に孤立させるような電位障壁を形成する電圧を印加することを特徴とする撮像素子を用いた測距方法。
【請求項８】
請求項７において、前記特定の感光部と前記電位障壁が形成される感光部の表面には遮光部が形成されていることを特徴とする撮像素子を用いた測距方法。
【請求項９】
受光量に応じて信号電荷を発生せしめる感光部と、感光部で発生した信号電荷を蓄積する蓄積部と、感光部から蓄積部への信号電荷の移送を開閉する電気スイッチとを備えるセンサ要素を半導体基板上に１次元または２次元的に配列すると共に、各センサ要素の蓄積部から蓄積電荷を読み出す転送部を前記半導体基板に形成し、前記半導体基板の特定の電極への電圧印加により前記電気スイッチを高周波で開閉できる構造を有する撮像素子と、
強度変調された光により照射された被検出物からの反射光を前記撮像素子のセンサ要素が配列された面に結像せしめる結像光学系と、
前記強度変調された光の変調信号に同期して、前記電気スイッチを閉じるための制御電圧を前記半導体基板の前記特定の電極に印加する同期積分制御部と、前記強度変調の複数の周期にわたって前記撮像素子の蓄積部に蓄積された電荷を前記転送部により読み出して測定値として記憶する記憶部と、
前記強度変調の一周期のうち前記電気スイッチを閉じるための制御電圧が印加される同期積分期間の位相を前記記憶部に測定値が記憶されるたびに切り替える検出位相設定部と、
記憶部に記憶された同期積分期間の位相が異なる複数の測定値に基づいて、各センサ要素ごとに被検出物までの距離情報を演算する測距演算部とを有することを特徴とする撮像素子を用いた測距装置。
【請求項１０】
請求項９において、前記蓄積部に蓄積された信号電荷を隣接する蓄積部に順次転送するための転送電極を前記蓄積部の表面に形成することにより前記転送部を構成すると共に、前記転送電極に信号電荷を転送するための電圧が印加されていない期間において、前記転送電極に前記感光部で発生した信号電荷を前記蓄積部に移送させる電圧と前記感光部で発生した信号電荷を前記蓄積部に移送させない電圧とを交互に印加することにより、前記感光部から蓄積部への信号電荷の移送を高周波で開閉する電気スイッチを構成したことを特徴とする撮像素子を用いた測距装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は撮像素子を用いた測距装置および測距方法に関するものであり、照射光に対する反射光の位相の遅れを撮像素子の各画素ごとに検出して被検出物の立体構造を検出可能とする技術に関するものである。
【０００２】
【従来の技術】
図３は従来のＴＯＦ（Ｔｉｍｅ　Ｏｆ　Ｆｌｉｇｈｔ）方式の光波測距の原理説明図である。図中、１は光源、２は被検出物、３は結像光学系、４は撮像素子である。光源１は例

えばＬＥＤアレイで構成されており、その出力光は高周波で強度変調されている。光源１に複数のＬＥＤを用いているのは、出力光の強度を増大させるためであり、各ＬＥＤは同期して発光している。光源１から被検出物２に照射される光が例えば２０ＭＨｚの高周波で強度変調されている場合、その波長は１５ｍとなるから、光が７．５ｍの距離を往復すれば１周期の位相の遅れが生じることになる。

【０００３】

照射光に対する反射光の位相の遅れについて図４により説明する。図中、Ｗは照射光、Ｒは反射光であり、反射光にはΨの位相遅れが生じている。照射光Ｗの１周期について４回、反射光Ｒをサンプリングして、照射光の位相が０°、９０°、１８０°、２７０°であるときの反射光の検出値をそれぞれＡ０，Ａ１，Ａ２，Ａ３とすると、位相の遅れΨは次式で与えられる。

Ψ＝ａｒｃｔａｎ｛（Ａ３－Ａ１）／（Ａ０－Ａ２）｝

【０００４】

被検出物２で反射された光は結像光学系３を介して撮像素子４の受光面に結像される。撮像素子４の受光面には複数の画素（Ｘ，Ｙ）が２次元的に配列されており、各画素について上式による位相遅れΨ（Ｘ，Ｙ）を求めることにより、被検出物２の立体的な構造を検出できる。

【０００５】

このＴＯＦ方式の光波測距に用いる撮像素子は、照射光の１周期について複数回のサンプリングができるものでなければならず、従来、特表平１０－５０８７３６号には図５あるいは図６のような構造が提案されている。図５の撮像素子は、１画素について１つの感光部ＰＤと４つのメモリーセルＭ０，Ｍ１，Ｍ２，Ｍ３を備え、各メモリーセルＭ０，Ｍ１，Ｍ２，Ｍ３と感光部ＰＤの間には時分割的にオンされる電気スイッチＳ０，Ｓ１，Ｓ２，Ｓ３が設けられている。各電気スイッチＳ０，Ｓ１，Ｓ２，Ｓ３はそれぞれ図４のＴ０，Ｔ１，Ｔ２，Ｔ３の期間でオンされる。この動作を複数周期にわたり繰り返すことにより、暗電流ノイズやショットノイズ（電子－正孔対の発生ばらつきによるノイズ）、アンプ回路の定常ノイズ等に対するＳ／Ｎ比を向上させることができ、反射光の検出値Ａ０，Ａ１，Ａ２，Ａ３がメモリーセルＭ０，Ｍ１，Ｍ２，Ｍ３に蓄積される。このような動作を、「同期積分」と呼ぶことにする。図６の撮像素子はデータ読み出し用のシフトレジスタＳＲを備え、時分割的にオンされる４つの電気スイッチＳ０，Ｓ１，Ｓ２，Ｓ３を介して１つの感光部ＰＤからシフトレジスタＳＲの各メモリーセルＭ０，Ｍ１，Ｍ２，Ｍ３に受光信号が蓄積され、シフトレジスタＳＲの転送機能により受光信号が読み出される。

【０００６】

【発明が解決しようとする課題】

しかしながら、上述の図５または図６に示すような特殊な構造を有する撮像素子をわざわざ製作するのでは製造コストが高くなり、測距装置全体のコストが上昇する。そこで、一般的なＣＣＤ撮像素子の制御方法を工夫することで、同期積分を実現できないか、種々検討したところ、ＣＣＤ撮像素子のオーバーフロードレイン電極あるいは垂直転送電極に印加する電圧を巧妙に制御することで実質的に同期積分しているのと同じような動作が実現できることを見出した。

【０００７】

本発明は、このような知見に基づいてなされたものであり、一般的なＣＣＤ撮像素子の制御方法を工夫することで、実質的に同期積分をしているのと同じような動作を実現可能とし、従来、特殊な構造の撮像素子を必要としていた光波測距を一般的なＣＣＤ撮像素子を用いて安価に実現することを課題とする。

【０００８】

【課題を解決するための手段】

本発明の測距装置は、上記の課題を解決するために、図１に示すように、複数の感光部を半導体基板上に１次元または２次元的に配列され、前記半導体基板への電圧印加により前記各感光部の感度を制御可能な構造を有する撮像素子４と、強度変調された光の変調信号

に同期して前記撮像素子４の半導体基板に前記各感光部の感度を変調せしめる電圧を印加する感度制御部５とを有することを特徴とするものである。より具体的には、強度変調された光により照射された被検出物２からの反射光を撮像素子４のセンサ要素が配列された面に結像せしめる結像光学系３と、前記強度変調された光の変調信号に同期して、撮像素子４の感光部の感度を低下させるための制御電圧を撮像素子４の半導体基板に印加する感度制御部５と、前記強度変調の複数の周期にわたって前記撮像素子４の蓄積部に蓄積された電荷を転送部により読み出して測定値として記憶する記憶部６と、前記強度変調の一周期のうち感光部の感度を低下させるための制御電圧が印加される低感度期間の位相を前記記憶部６に測定値が記憶されるたびに切り替える検出位相設定部７と、記憶部６に記憶された低感度期間の位相が異なる複数の測定値に基づいて、撮像素子４の各センサ要素ごとに被検出物２までの距離情報を演算する測距演算部８とを有することを特徴とするものである。

【０００９】

ここで、本発明の測距装置に用いる撮像素子４は、図１（ｂ）に示すように、受光量に応じて信号電荷を発生せしめる感光部ＰＤと、感光部ＰＤで発生した信号電荷を蓄積する蓄積部Ｍと、感光部ＰＤから蓄積部Ｍへの信号電荷の移送を開閉する電気スイッチＳとを備えるセンサ要素を半導体基板上に１次元または２次元的に配列すると共に、各センサ要素の蓄積部Ｍから蓄積電荷を読み出す転送部Ｔを前記半導体基板に形成し、前記半導体基板の特定の電極（例えば転送電極）への電圧印加により前記電気スイッチＳを高周波で開閉できる構造を有する撮像素子とするか、あるいは、図１（ｃ）に示すように、前記電気スイッチＳを高周波では開閉できないが、これをオンにしたままで、前記半導体基板の他の特定の電極（例えばオーバーフロードレーン電極）への電圧印加により感度を高周波で増減させることができる感度可変感光部ＰＤ’を有するような撮像素子とする。具体的には、縦型または横型オーバーフロードレイン電極を有するインターライン・トランスファ型ＣＣＤ撮像素子、あるいは、縦型または横型オーバーフロードレイン電極を有するフレーム・トランスファ型ＣＣＤ撮像素子、もしくは、これらの複合型であるフレーム・インターライン・トランスファ型ＣＣＤ撮像素子が利用できる。

【００１０】

図２は本発明の動作説明図である。図中、（ａ）は照射光Ｗの位相を示しており、（ｂ）～（ｅ）は検出位相設定部７で設定される同期積分のための検出位相を示している。従来の技術では、１つのセンサ要素ごとに、図５または図６に示すように、１つの感光部ＰＤと複数のスイッチＳ０～Ｓ３と複数のメモリーセルＭ０～Ｍ３を設けて、スイッチＳ０、Ｓ１、Ｓ２、Ｓ３をそれぞれ図２（ｂ）、（ｃ）、（ｄ）、（ｅ）の検出位相で時分割的にオンさせていた。本発明では、図１（ｂ）に示すように、１つのセンサ要素ごとに、受光量に応じて信号電荷を発生せしめる感光部ＰＤと、感光部ＰＤで発生した信号電荷を蓄積する蓄積部Ｍと、感光部ＰＤから蓄積部Ｍへの信号電荷の移送を開閉する電気スイッチＳとを１つずつ備え、１回目の撮像時には電気スイッチＳを図２（ｂ）の検出位相で繰り返しオンすることにより、蓄積部Ｍに図４のＡ０に相当する測定値を得て、これを転送部Ｔにより１画面分、読み出す。２回目、３回目、４回目の撮像時には電気スイッチＳをそれぞれ図２（ｃ）、（ｄ）、（ｅ）の検出位相で繰り返しオンすることにより、蓄積部Ｍに図４のＡ１、Ａ２、Ａ３に相当する測定値を得て、これを１画面分ずつ、転送部Ｔにより読み出す。以上の動作を制御回路９により統括制御する。このようにすれば、図５または図６に示す構造の撮像素子を用いる場合に比べて４倍の測定時間を要するものの、被検出物２が高速で移動しなければ、検出位相の異なる４枚の画像を取得することができ、一般的なＣＣＤ撮像素子を用いても光波測距が実現できる。なお、測距演算部８は実質的に距離情報を演算できるものであれば良く、マイコン、ＤＳＰ、演算増幅器等、任意の手段で構成できる。

【００１１】

ところで、ＣＣＤ撮像素子として最も一般的なインターライン・トランスファ型のＣＣＤ撮像素子において、図１（ｂ）の電気スイッチＳを構成する電極は垂直転送電極と兼用さ

れており、この電極は半導体基板上に絶縁薄膜を介して形成されているので、形状の割りには静電容量が大きく、容量が大きい場合は、数十ＭＨｚの高周波で開閉することは極めて困難であることが分かった。このような場合は、一般的なＣＣＤ撮像素子を用いて近距離の光波測距を実現する用途には不向きである。

【００１２】

そこで、図１（ｃ）に示すように、感光部と蓄積部の間の電気スイッチＳはＯＮ状態に維持したままで、感光部の感度のみを照射光と同期して周期的に低下させることができる手段が無いか検討した。感光部の感度とは、要するに受光量に対する光電子の発生効率のことであるから、発生した光電子の一部を捨てることができれば、実質的には感度が低下していることになる。

【００１３】

このような感光部の光電子を捨てる手段として、ＣＣＤ撮像素子のなかには、過剰な信号電荷を基板に捨てるためのオーバーフロードレインと呼ばれる構造を有するものがある。このオーバーフロードレインは、もともとは感光部に強過ぎる光が入手したときに、発生した過剰な信号電荷が周囲の感光部に影響を及ぼすのを防ぐために、所定のレベルを越える信号電荷を基板に捨てるために設けられたものであるが、このオーバーフロードレインが信号電荷をオーバーフローさせるレベルを意図的に下げてやれば、感光部の信号電荷が過剰でなくても信号電荷は過剰であるものとして捨てられることになり、実質的に感光部の感度を低下させることができる。しかも、このオーバーフロードレインは基板に直結されているので、形状の割りには静電容量が小さく、数十ＭＨｚでのスイッチングも可能である。そこで、光を検出したくない位相ではオーバーフロードレインが信号電荷をオーバーフローさせるレベルを低く設定してやれば、感光部の感度を照射光の周期に合わせて変調することができる。

【００１４】

もちろん、このオーバーフロードレイン電極をＣＣＤカメラの電子シャッターに利用するという考え方は従来から存在するが、それは１回切りの露光を意図したものであったので、蓄積部の電荷が初期化された状態から積分を開始するものであった。蓄積部の電荷を初期化せずに、前回までの露光による残像を残したままで複数回の露光をオーバーフロードレイン電極の印加電圧制御により実現するような制御方法は知られていない。

【００１５】

以下、発明の実施の形態として、縦型または横型オーバーフロードレイン電極を有するインターライン・トランスファ型ＣＣＤ撮像素子ならびにフレーム・トランスファ型ＣＣＤ撮像素子について、同期積分と同じような動作を実現するための具体的な制御方法について詳しく説明する。

【００１６】

【発明の実施の形態】

（実施の形態１）

図７は縦型オーバーフロードレイン（ＶＯＤ）電極を有するインターライン・トランスファ型ＣＣＤ（ＩＴ－ＣＣＤ）の構成を示している。ｎ型基板１０の表面には、アルミニウム電極よりなる縦型オーバーフロードレイン（ＶＯＤ）電極１１が絶縁膜を介さず基板に直接接触するように形成されている。ＶＯＤ電極１１には制御電圧Ｖｓが印加されている。ｎ型基板１０の表面のＶＯＤ電極１１で囲まれた部分にはｐ型領域１２が形成されている。このｐ型領域１２に複数のフォトダイオードが分離して形成されている。図中、ＰＤと記した部分はフォトダイオードであり、このフォトダイオードＰＤが形成された部分以外の表面は遮光膜（図示せず）で覆われている。図７では垂直方向に３列、水平方向に４行のフォトダイオードＰＤを図示しているが、実際にはより多数のフォトダイオードＰＤが形成されている。各フォトダイオードＰＤに隣接して形成された電極ａ，ｂ，ｃ，ｄならびにａ’，ｂ’，ｃ’，ｄ’は垂直転送ＣＣＤの電極であり、この電極の下にフォトダイオードＰＤで発生した信号電荷を蓄積し、蓄積された信号電荷を４相の垂直転送電圧Ｖ１，Ｖ２，Ｖ３，Ｖ４により水平転送ＣＣＤに転送する。（各列のフォトダイオードＰＤ

に隣接して形成された垂直転送ＣＣＤの電極は、水平方向に並んだ電極に同じ垂直転送電圧が印加されるように図示しない配線を介して接続されている。）水平転送ＣＣＤは２相の水平転送電圧ＶＨ１，ＶＨ２により電荷を転送するための水平転送電極ｅ，ｆ，ｅ’，ｆ’，ｅ”，ｆ”を備えている。ＩＴ－ＣＣＤでは、垂直転送は４相クロック、水平転送は２相クロックで行うことが極めて一般的であり、その電荷転送の仕組みについては周知のものであるので、詳しい説明は省略する。

【００１７】

図８はフォトダイオードＰＤと垂直転送電極ａ，ｂの部分の断面構造を示している。上述のように、ｎ型基板１０の表面には、ｐ型領域１２が形成されており、このｐ型領域１２の表面には、複数のフォトダイオードＰＤが形成されている。各フォトダイオードＰＤはｎ＋領域１３とｐ型領域１２とから構成されている。フォトダイオードＰＤの表面にはｐ＋層１４が形成されている。このｐ＋層１４の効果について説明すると、基板表面の結晶構造は結晶性が悪く、エネルギーの安定性が悪い（エネルギーが活性である）ので、熱励起により電子－正孔対が発生し易く、これが暗電流となって信号電荷のＳ／Ｎ比を悪くする一因となる。この影響を防ぐために、信号電荷が表面付近を通らないようにすることが、ｐ＋層１４の役割であり、この構造を有するフォトダイオードは、埋め込みフォトダイオードなどと呼ばれている。各フォトダイオードＰＤに隣接して、ｐ型領域１２の表面に垂直転送ＣＣＤを構成するｎ層１５が形成されている。このｎ層１５の表面には、SiO_2 よりなる絶縁薄膜１６を介して、ポリシリコンゲート電極よりなる垂直転送電極ａ，ｂが形成されている。このポリシリコンゲート電極は絶縁薄膜１６を介して形成されているので、形状の割りに静電容量が大きく、静電容量が大きい場合は、数十ＭＨｚの高周波でスイッチングすることは困難である。なお、フォトダイオードＰＤと垂直転送電極ｃ，ｄの部分の断面構造も図８と同様である。

【００１８】

図９は図８のＡ－Ａ’線について垂直転送ＣＣＤの垂直転送電極ａ，ｂ，ｃ，ｄの断面構造を示している。第１の垂直転送電極ａ，ｃはフォトダイオードＰＤから垂直転送ＣＣＤへの電荷読み出しと垂直転送の役割を果たす。第２の垂直転送電極ｂ，ｄは垂直転送の役割を果たす。垂直転送電極ａ，ｂ，ｃ，ｄの上部には遮光膜１７が形成されている。

【００１９】

図１０は図８の太い破線に沿って電子のポテンシャルを示している。つまり、垂直転送ＣＣＤのｎ層１５からｐ＋層１４’（厳密には基板表面のｐ＋層１４とは別工程で形成されている）、フォトダイオードＰＤのｎ＋層１３、ｐ型領域１２、ｎ型基板１０に沿って電子のポテンシャルを示したものである。フォトダイオードＰＤと垂直転送ＣＣＤの間のｐ＋層１４の電位障壁（図１０の右側の破線で示す）は垂直転送電極ａ，ｃの印加電圧を高くすることにより崩すことができる。また、フォトダイオードＰＤとｎ型基板１０の間のｐ型領域１２の電位障壁（図１０の左側の破線で示す）はＶＯＤ電極１１の印加電圧を高くすることにより崩すことができる。図中の白丸に－（マイナス）の記号を付したものは光電子を意味している。また、フォトダイオードＰＤの部分の光電子で“たてがみ”のような模様を周囲に付したものは、光電変換により発生した光電子を意味している。以下の説明においても同様である。

【００２０】

ＩＴ－ＣＣＤにおいて、ＶＯＤ電極を設けている本来の理由は、フォトダイオードＰＤに非常に強い光が入射したときに、過剰な信号電荷をｎ型基板１０に逃がすためであるが、本発明では、信号電荷が過剰でなくても、フォトダイオードＰＤの感度を下げたいときには、信号電荷が過剰であることにして、基板にオーバーフローさせてしまうことにより、フォトダイオードＰＤの感度を可変としている。すなわち、フォトダイオードＰＤの感度を低下させたいときには、ＶＯＤ電極１１に高い＋電圧を印加することにより、フォトダイオードＰＤのｎ＋層１３とｎ型基板１０の間のｐ型領域１２の電位障壁を下げてフォトダイオードＰＤの発生電荷をｎ型基板１０に逃がすようにしている。フォトダイオードＰＤと垂直転送ＣＣＤの間にもｐ＋層１４’の電位障壁が存在するが、第１の垂直転送電極

ａに所定の＋電圧を印加しておくことによりｐ＋層１４’の電位障壁を下げてフォトダイオードＰＤに発生した電荷を垂直転送電極ａの下に集めることができる。ＶＯＤ電極１１に高い＋電圧が印加されている場合には、フォトダイオードＰＤで発生した電荷は垂直転送ＣＣＤにも少しは流れるが、主に比較的電子のポテンシャルが低いｎ型基板１０の方に捨てられることになるので、フォトダイオードＰＤの感度（光電変換効率）は実質的に低下する。この光電子廃棄期間を同期積分休止期間（非検出位相）とする。また、ＶＯＤ電極１１の印加電圧を低下させて光電子の廃棄をやめると、フォトダイオードＰＤで発生した電荷は垂直転送ＣＣＤに効率良く流れて、垂直転送電極の下に蓄積されることになる。この光電子蓄積期間を同期積分期間（検出位相）とする。

【００２１】

ＶＯＤ型ＩＴ－ＣＣＤによる光電子の蓄積、廃棄、読み出しの各期間の動作を図１１に示し説明する。光電子の蓄積期間では、ＶＯＤ電極１１の印加電圧は低く、また、フォトダイオードＰＤの隣に形成されている垂直転送電極ａには十分高い電圧Ｖ１を与えて、図１１（ａ）に示すように、垂直転送電極下のｎ層１５のポテンシャルを下げるとともに、ｎ層１５とｎ＋層１３との間に形成されているｐ＋層１４’による電位障壁を崩す。これは図１（ｃ）の電気スイッチＳが閉じていることに相当する。この場合、ｎ＋層１３で発生した光電子は垂直転送電極下のｎ層１５に蓄積される。

【００２２】

光電子の廃棄期間では、ｎ型基板１０に接続されたＶＯＤ電極１１に高い＋電圧Ｖｓを印加し、ｎ型基板１０のポテンシャルを下げる。印加電圧Ｖｓが十分高い場合、図１１（ｂ）に示すように、ｎ型基板１０とｎ＋層１３の間に形成されたｐ型領域１２による電位障壁が崩れ、ｎ＋層１３で発生した光電子の多くはｎ型基板１０に廃棄される。このとき、垂直転送電極ａには、光電子の蓄積期間と同様、電圧Ｖ１を印加したままにしておく。これは図１（ｃ）の電気スイッチＳが閉じたままであることに相当する。垂直転送電極下のｎ層１５のポテンシャルよりもｎ型基板１０のポテンシャルの方が低くなるようにＶＯＤ電極１１の印加電圧Ｖｓを設定すると、ｎ＋層１３で発生した光電子はポテンシャルの低い方へ引き寄せられるため、大部分は垂直転送電極ａ側へ行くことなく、ＶＯＤ電極１１（ｎ型基板１０）へ廃棄される。また、光電子の蓄積期間中に垂直転送電極下のｎ層１５に蓄積された光電子は、ｎ＋層１３の電位障壁があるため、ＶＯＤ電極１１（ｎ型基板１０）側に廃棄されることはない。

【００２３】

光電子の蓄積期間（図１１（ａ））と光電子の廃棄期間（図１１（ｂ））とは照射光の一周期内で交番し、例えば図２（ｂ）のように、特定の検出位相（同期積分期間）でのみ光電子の蓄積を行い、残りの非検出位相（積分休止期間）では（蓄積部の光電子は残したまま感光部で発生する）光電子を廃棄する。この動作を照射光の複数の周期にわたり繰り返すことにより、図４のＡ０に相当する検出値が各画素ごとに得られる。この検出値をひとまず読み出す。

【００２４】

蓄積された光電子の読み出し期間では、図１１（ｃ）に示すように、垂直転送ＣＣＤのｎ層１５とフォトダイオードＰＤのｎ＋層１３との間にｐ＋層１４’による電位障壁を発生させるように、垂直転送電極ａの電圧Ｖ１を低く設定し、転送電圧Ｖ１～Ｖ４に４相の転送クロックを与えて、蓄積された信号電荷を読み出す。これは、図１（ｂ）の電気スイッチＳが開いた状態に相当する。

【００２５】

このようにして、図４のＡ０に相当する検出値が各画素ごとに得られると、次に、図２（ｃ）のように、検出位相を９０度ずらして、光電子の蓄積と廃棄を照射光の複数の周期にわたり繰り返すことにより、図４のＡ１に相当する検出値が各画素毎に得られる。この検出値を読み出すと、今度は図２（ｄ）、さらには図２（ｅ）のように、検出位相を１８０度、２７０度というようにずらして行き、光電子の蓄積と廃棄を照射光の複数の周期にわたり繰り返すことにより、図４のＡ２、Ａ３に相当する検出値が各画素毎に得られる。な

お、各回の同期積分の回数は同じにすることは言うまでも無い。

【００２６】

検出位相をずらす順番は上記に限定されるものではない。たとえば、測距演算の計算式：Ψ＝ａｒｃｔａｎ｛（Ａ３－Ａ１）／（Ａ０－Ａ２）｝に合わせて、最初にＡ３の検出値を求めて第１の画像メモリに蓄積し、次にＡ１の検出値を求めて（Ａ３－Ａ１）を同じ第１の画像メモリに上書きする。次に、Ａ０の検出値を求めて第２の画像メモリに蓄積し、さらにＡ２の検出値を求めて（Ａ０－Ａ２）を同じ第２の画像メモリに上書きする。というようにすれば、画像メモリの記憶容量は半分で済むことになる。

【００２７】

また、検出位相は必ずしも図２（ｂ）～（ｅ）のように一周期中の限られた狭い期間とする必要はなく、Ｓ／Ｎ比を高めるために、検出位相を広くしても構わない。例えば、一周期中の半分を検出位相、残りの半分を非検出位相として測定した第１の画像と、この第１の画像とは検出位相と非検出位相を入れ替えて測定した第２の画像とを比較するだけでも遠近の情報は得ることができる。

【００２８】

さらに、強度変調された照射光についても、振幅が正弦波である必要はなく、矩形波や三角波で強度変調されていても構わない。

また、強度変調された照射光は可視光である必要はなく、目に見えない近赤外光とすれば、夜間の監視用途などに利用できる。

【００２９】

ところで、縦型オーバーフロードレイン電極を有するＣＣＤは、フォトダイオードＰＤの受光面積を大きくできる半面、フォトダイオードＰＤのｎ＋領域を深くまで形成できないので、近赤外光に対する感度が低くなる欠点がある。そこで、この欠点を解消するために、フォトダイオードＰＤのｎ＋領域を深くまで形成できる横型オーバーフロードレイン（ＬＯＤ）電極を有するＩＴ－ＣＣＤについて次に説明する。

【００３０】

（実施の形態２）

図１２は横型オーバーフロードレイン（ＬＯＤ）を有するインターライン・トランスファ型ＣＣＤ（ＩＴ－ＣＣＤ）の構成を示している。ｐ型基板２２の表面には、垂直方向に複数本のｎ型領域２０が形成されており、各ｎ型領域２０は、アルミニウム電極よりなるＬＯＤ電極２１に接続されている。ＬＯＤ電極２１には制御電圧Ｖｓが印加されている。各ｎ型領域２０に隣接してｐ型基板２２の表面に複数のフォトダイオードが分離して形成されている。図中、ＰＤと記した部分はフォトダイオードであり、このフォトダイオードＰＤが形成された部分以外の表面は遮光膜で覆われている。図１２では垂直方向に３列、水平方向に４行のフォトダイオードＰＤを図示しているが、実際にはより多数のフォトダイオードＰＤが形成されている。各フォトダイオードＰＤに隣接して形成された電極ａ，ｂ，ｃ，ｄならびにａ’，ｂ’，ｃ’，ｄ’は垂直転送ＣＣＤの電極であり、この電極の下にフォトダイオードＰＤで発生した信号電荷を蓄積し、蓄積された信号電荷を４相の垂直転送電圧Ｖ１，Ｖ２，Ｖ３，Ｖ４により水平転送ＣＣＤに転送する。（各列のフォトダイオードＰＤに隣接して形成された垂直転送ＣＣＤの電極は、水平方向に並んだ電極に同じ垂直転送電圧が印加されるように図示しない配線を介して接続されている。）水平転送ＣＣＤは２相の水平転送電圧ＶＨ１，ＶＨ２により電荷を転送するための水平転送電極ｅ，ｆ，ｅ’，ｆ’，ｅ”，ｆ”を備えている。ＩＴ－ＣＣＤでは、垂直転送は４相クロック、水平転送は２相クロックで行うことが極めて一般的であり、その電荷転送の仕組みについては周知のものであるので、詳しい説明は省略する。

【００３１】

図１３はフォトダイオードＰＤと垂直転送電極ａ，ｂの周辺の断面構造を示している。上述のように、ｐ型基板２２の表面には、ＬＯＤ電極２１に接続されたｎ型領域２０が形成されており、このｎ型領域２０に隣接してフォトダイオードＰＤが形成されている。各フォトダイオードＰＤはｎ＋領域２３とｐ型基板２２とから構成されている。フォトダイオ

ードＰＤの表面にはｐ＋層２４が形成されている。このｐ＋層２４の効果について説明すると、基板表面の結晶構造は結晶性が悪く、エネルギーの安定性が悪い（エネルギーが活性である）ので、熱励起により電子－正孔対が発生し易く、これが暗電流となって信号電荷のＳ／Ｎ比を悪くする一因となる。この影響を防ぐために、信号電荷が表面付近を通らないようにすることが、ｐ＋層２４の役割であり、この構造を有するフォトダイオードは、埋め込みフォトダイオードなどと呼ばれている。各フォトダイオードＰＤに隣接して、ｐ型基板２２の表面に垂直転送ＣＣＤを構成するｎ層２５が形成されている。このｎ層２５の表面には、SiO_2 よりなる絶縁薄膜２６を介して、ポリシリコンゲート電極よりなる垂直転送電極ａ，ｂが形成されている。このポリシリコンゲート電極は絶縁薄膜２６を介して形成されているので、形状の割りに静電容量が大きく、静電容量が大きい場合は数十ＭＨｚの高周波でスイッチングすることは困難である。なお、フォトダイオードＰＤと垂直転送電極ｃ，ｄの周辺の断面構造も図１３と同様である。

【００３２】
図１３のＡ－Ａ’線についての断面構造は図９と同じである。第１の垂直転送電極ａ，ｃはフォトダイオードＰＤから垂直転送ＣＣＤへの電荷読み出しと垂直転送の役割を果たす。第２の垂直転送電極ｂ，ｄは垂直転送の役割を果たす。垂直転送電極ａ，ｂ，ｃ，ｄの上部には遮光膜２７が形成されている。また、ＬＯＤ電極２１に接続されたｎ型領域２０の上部にも遮光膜２７が形成されている。

【００３３】
図１４は図１３の太い破線に沿って電子のポテンシャルを示している。つまり、垂直転送ＣＣＤのｎ層２５からｐ＋層２４’（厳密には基板表面のｐ＋層２４とは別工程で形成されている）、フォトダイオードＰＤのｎ＋層２３、ｐ＋層２４’、ＬＯＤ電極２１に接続されたｎ型領域２０に沿って電子のポテンシャルを示したものである。フォトダイオードＰＤと垂直転送ＣＣＤの間のｐ＋層２４’の電位障壁（図１４の右側の破線で示す）は垂直転送電極ａ，ｃの印加電圧を高くすることにより崩すことができる。また、フォトダイオードＰＤとｎ型領域２０の間のｐ＋層２４’の電位障壁（図１４の左側の破線で示す）はＬＯＤ電極２１の印加電圧を高くすることにより崩すことができる。

【００３４】
ＬＯＤ型のＩＴ－ＣＣＤにおいて、ＬＯＤ電極を設けている本来の理由は、フォトダイオードＰＤに非常に強い光が入射したときに、過剰な信号電荷をフォトダイオードＰＤに隣接するｎ型領域２０に逃がすためであるが、本発明では、信号電荷が過剰でなくても、フォトダイオードＰＤの感度を下げたいときには、信号電荷が過剰であることにして、ｎ型領域２０にオーバーフローさせてしまうことにより、フォトダイオードＰＤの感度を可変としている。すなわち、フォトダイオードＰＤの感度を低下させたいときには、ＬＯＤ電極２１に高い＋電圧を印加することにより、フォトダイオードＰＤのｎ＋層２３とｎ型領域２０の間のｐ＋層２４’の電位障壁を下げてフォトダイオードＰＤの発生電荷をｎ型領域２０に逃がすようにしている。フォトダイオードＰＤと垂直転送ＣＣＤの間にもｐ＋層２４’の電位障壁が存在するが、第１の垂直転送電極ａに所定の＋電圧を印加しておくことによりｐ＋層２４’の電位障壁を下げてフォトダイオードＰＤに発生した電荷を垂直転送電極ａの下に集めることができる。ＬＯＤ電極２１に高い＋電圧が印加されている場合には、フォトダイオードＰＤで発生した電荷は垂直転送ＣＣＤにも少しは流れるが、主にｎ型領域２０の方に捨てられることになるので、フォトダイオードＰＤの感度（光電変換効率）は実質的に低下する。この光電子廃棄期間を同期積分休止期間（非検出位相）とする。また、ＬＯＤ電極２１の印加電圧を低下させて光電子の廃棄をやめると、フォトダイオードＰＤで発生した電荷は垂直転送ＣＣＤに効率良く流れて、垂直転送電極の下に蓄積されることになる。この光電子蓄積期間を同期積分期間（検出位相）とする。

【００３５】
ＬＯＤ型ＩＴ－ＣＣＤによる光電子の蓄積、廃棄、読み出しの各期間の動作を図１５に示し説明する。光電子の蓄積期間では、ＬＯＤ電極２１の印加電圧は低く、また、フォトダイオードＰＤの隣に形成されている垂直転送電極ａに十分高い電圧Ｖ１を与えて、図１５

（ａ）に示すように、垂直転送電極下のｎ層２５のポテンシャルを下げるとともに、ｎ層２５とｎ＋層２３との間に形成されているｐ＋層２４’による電位障壁を崩す。これは図１（ｃ）の電気スイッチＳが閉じていることに相当する。この場合、ｎ＋層２３で発生した光電子は垂直転送電極下のｎ層２５に蓄積される。

【００３６】

光電子の廃棄期間では、ｎ型領域２０に接続されたＬＯＤ電極２１に高い＋電圧Ｖｓを印加し、ｎ型領域２０のポテンシャルを下げる。印加電圧Ｖｓが十分高い場合、図１５（ｂ）に示すように、ｎ型領域２０とｎ＋層２３の間に形成されたｐ＋層２４’による電位障壁が崩れ、ｎ＋層２３で発生した光電子の多くはｎ型領域２０に廃棄される。このとき、垂直転送電極ａには、光電子の蓄積期間と同様、電圧Ｖ１を印加したままにしておく。これは図１（ｃ）の電気スイッチＳが閉じたままであることに相当する。垂直転送電極下のｎ層２５のポテンシャルよりもｎ型領域２０のポテンシャルの方が低くなるようにＬＯＤ電極２１の印加電圧Ｖｓを設定すると、ｎ＋層２３で発生した光電子はポテンシャルの低い方へ引き寄せられるため、大部分は垂直転送電極ａ側へ行くことなく、ｎ型領域２０を介してＬＯＤ電極２１へ廃棄される。また、光電子の蓄積期間中に垂直転送電極下のｎ層２５に蓄積された光電子は、ｎ＋層２３の電位障壁があるため、ＬＯＤ電極２１（ｎ型領域２０）側に廃棄されることはない。

【００３７】

光電子の蓄積期間（図１５（ａ））と光電子の廃棄期間（図１５（ｂ））とは照射光の一周期内で交番し、例えば図２（ｂ）のように、特定の検出位相（同期積分期間）でのみ光電子の蓄積を行い、残りの非検出位相（積分休止期間）では光電子を廃棄する。この動作を照射光の複数の周期にわたり繰り返すことにより、図４のＡ０に相当する検出値が各画素ごとに得られる。この検出値をひとまず読み出す。

【００３８】

蓄積された光電子の読み出し期間では、図１５（ｃ）に示すように、垂直転送ＣＣＤのｎ層２５とフォトダイオードＰＤのｎ＋層２３との間にｐ＋層２４’による電位障壁を発生させるように、垂直転送電極ａの電圧Ｖ１を低く設定し、転送電圧Ｖ１～Ｖ４に４相の転送クロックを与えて、蓄積された信号電荷を読み出す。これは、図１（ｂ）の電気スイッチＳが開いた状態に相当する。

【００３９】

このようにして、図４のＡ０に相当する検出値が各画素ごとに得られると、次に、図２（ｃ）のように、検出位相を９０度ずらして、光電子の蓄積と廃棄を照射光の複数の周期にわたり繰り返すことにより、図４のＡ１に相当する検出値が各画素毎に得られる。この検出値を読み出すと、今度は図２（ｄ）、さらには図２（ｅ）のように、検出位相を１８０度、２７０度というようにずらして行き、光電子の蓄積と廃棄を照射光の複数の周期にわたり繰り返すことにより、図４のＡ２、Ａ３に相当する検出値が各画素毎に得られる。なお、各回の同期積分の回数は同じにすることは言うまでも無い。

【００４０】

ところで、横型オーバーフロードレイン電極を有するＩＴ－ＣＣＤでは、フォトダイオードＰＤを形成するｎ＋領域２３をｐ型基板２２の深くまで形成することができるので、近赤外線に対する検出感度を高めることができる利点がある。その半面、フォトダイオードＰＤに隣接してＬＯＤ電極２１に接続されたｎ型領域２０を設ける面積が必要であり、その分、フォトダイオードＰＤの受光面積が狭くなるので、開口率が減少する欠点がある。また、ＩＴ－ＣＣＤでは、フォトダイオードＰＤに隣接して垂直転送ＣＣＤを設ける必要があるので、その分、フォトダイオードＰＤの受光面積は制限される。そこで、フォトダイオードＰＤそのものに転送機能を持たせて受光面積を広くしたＦＴ－ＣＣＤについて次に説明する。

【００４１】

（実施の形態３）

図１６は縦型オーバーフロードレイン（ＶＯＤ）電極を有するフレーム・トランスファ型

ＣＣＤ（ＦＴ－ＣＣＤ）の構成を示している。ｎ型基板３０の表面には、アルミニウム電極よりなる縦型オーバーフロードレイン（ＶＯＤ）電極３１が絶縁膜を介さず基板に直接接触するように形成されている。ＶＯＤ電極３１には制御電圧Ｖｓが印加されている。ｎ型基板３０の表面のＶＯＤ電極３１で囲まれた部分にはｐ型領域３２が形成されている。このｐ型領域３２には、複数本の垂直方向に長いｎ型領域３５が形成されている。図１６の破線で囲まれた部分は１画素分のフォトダイオードＰＤを構成しており、その断面構造を図１７に示す。

【００４２】

ｎ型領域３５の表面には、SiO_2 よりなる絶縁薄膜３６を介して、ｎ型領域３５の長手方向に沿って複数個のポリシリコンゲート電極ａ，ｂ，ｃが形成されている。各ポリシリコンゲート電極ａ，ｂ，ｃはｎ型領域３５の長手方向とは垂直方向に伸びるように形成されており、３個のゲート電極ａ，ｂ，ｃで一つの画素を構成している。図１６では限られた個数の画素しか図示していないが、実際には水平方向および垂直方向の解像度に応じた個数の画素が構成されるものである。

【００４３】

ポリシリコンゲート電極ａ，ｂ，ｃおよびSiO_2 よりなる絶縁薄膜３６は光を透過するので、ｎ型領域３５には光電子が発生する。ただし、図１６の撮像部以外の部分は遮光膜で覆われており、蓄積部や水平転送部には光電子は発生しない。蓄積部は垂直帰線期間中に撮像部の信号電荷を一括して高速転送され、蓄積部に蓄積された信号電荷を次回の垂直帰線期間までの間に水平転送部を介して読み出すものである。蓄積部のゲート電極に印加される電圧φ１～φ３は撮像部のゲート電極に印加される電圧Ｖ１～Ｖ６とは分離されており、蓄積部から水平転送部を介して画像信号を読み出している途中においても撮像部において信号電荷の蓄積が可能である。したがって、フレーム・トランスファ型ＣＣＤを用いると、インターライン・トランスファ型ＣＣＤを用いる場合に比べて同期積分の蓄積時間を長く取ることが可能となる。この例では、Ｖ１～Ｖ６の６相の転送電圧を用いて撮像部から蓄積部に信号電荷を転送可能としている。一方、蓄積部から水平転送部には、φ１～φ３の３相の転送電圧を用いて信号電荷を転送可能としている。（撮像部および蓄積部の各ゲート電極は、水平方向に並んだ電極に同じ転送電圧Ｖ１～Ｖ６、φ１～φ３が印加されるように図示しない配線を介して接続されている。）水平転送部は上述した水平転送ＣＣＤと同じものであるので、詳細な説明は省略するが、ここでもＶＨ１，ＶＨ２の２相の転送電圧を用いて信号電荷を転送可能としている。

【００４４】

図１８は図１７の破線に沿って電子のポテンシャルを示している。光電子が発生するｎ型領域３５とｎ型基板３０の間には、図１８の破線で示すように、ｐ型領域３２による電位障壁が存在するが、ｎ型基板３０に接続されたＶＯＤ電極３１に高い＋電圧を印加すると、この電位障壁を崩すことができ、ｎ型領域３５からｎ型基板３０に信号電荷（光電子）を捨てることができる。

【００４５】

光電子の蓄積期間では、ＶＯＤ電極３１の印加電圧Ｖｓは低くしておき、ｎ型領域３５とｎ型基板３０の間に、ｐ型領域３２による電位障壁が存在するようにしておく。また、図１９（イ）のように、１画素につき３枚のゲート電極ａ，ｂ，ｃを使用し、中央のゲート電極ｂに最も高い＋電圧を印加することでゲート電極ｂ下で発生した光電子のみならずゲート電極ａ、ｃ下で発生した光電子もゲート電極ｂ下のポテンシャル井戸に蓄積する。この様子を図１９（ハ）に示す。図１９（ハ）は図１９（イ）の太い一点鎖線についての電子のポテンシャルを示したものである。また、図１９（ニ）は図１９（ロ）の太い破線についての電子のポテンシャルを各ゲート電極ａ，ｂ，ｃについて示している。

【００４６】

光電子の廃棄期間では、ＶＯＤ電極３１に高い＋電圧を印加し、図１９（ニ）に示すように、ｎ型領域３５とｎ型基板３０の間のｐ型領域３２による電位障壁の高さを破線から実線に示すように下げる。このとき、ＶＯＤ電極３１に印加する電圧は、ｎ型基板３０のポ

テンシャルがゲート電極ｂ下のｎ型領域３５のポテンシャルよりも高く、且つゲート電極ａ、ｃ下のｎ型領域３５のポテンシャルよりも低くなるように設定する。ゲート電極ａ，ｂ，ｃに印加される電圧は、光電子の蓄積期間と同様であり、中央のゲート電極ｂには両側のゲート電極ａ，ｃよりも高い＋電圧が印加されているので、両側のゲート電極ａ，ｃの下ではｐ型領域３２による電位障壁は完全に崩されるが、中央のゲート電極ｂの下ではｐ型領域３２による電位障壁は高さが低くなるだけで完全には崩されない。このため、両側のゲート電極ａ，ｃの下で発生した光電子の多くはｎ型基板３０に廃棄されるが、中央のゲート電極ｂの下で発生した光電子は廃棄されないし、光電子の蓄積期間において中央のゲート電極ｂの下に蓄積された光電子も廃棄されない。

【００４７】

上述の光電子の蓄積と廃棄を複数回繰り返すと、中央のゲート電極ｂの下には、光電子の蓄積期間において両側のゲート電極ａ，ｂから中央のゲート電極ｂに蓄積された光電子が余分に蓄積されることになる。中央のゲート電極ｂは常に光電子を蓄積しているので、この常時積分による平均値が同期積分による検出値に加算されることになるが、それでも両側のゲート電極ａ，ｂから同期積分による検出値を得ているので、十分なコントラストを得ることができる。

【００４８】

また、例えば照射光の一周期のうち、半分を光電子の蓄積期間とし、残りの半分を光電子の廃棄期間として同期積分した画像を、照射光に対する光電子の蓄積期間の位相をずらしながら複数枚観測することによっても距離情報を算出することはできるので、この例のように光電子の蓄積期間が長い用途では、コントラストが高くなるからＦＴ－ＣＣＤを利用できる。

【００４９】

さらに、３枚のゲート電極に限らず、５枚、７枚といった多数枚のゲート電極で１画素を構成し、中央の１枚のゲート電極に光電子を集中させるようにすれば、周囲のゲート電極から集めた同期積分による検出値の成分が、中央のゲート電極における常時積分による平均値の成分よりも相対的に大きくなり、コントラストをさらに改善できる。

【００５０】

なお、縦型オーバーフロードレイン電極３１はｐ型領域３２の周囲のｎ型基板３０にｐ型領域３２を取り囲むようにアルミニウム電極を形成する必要があるので、ｐ型領域３２はエピタキシャル成長により形成することはできない。拡散法により形成した場合は、ｐ型領域をあまり深くまで形成できない。したがって、フォトダイオードとなるｎ型領域３５はｐ型領域３２よりもさらに浅く形成されることになり、近赤外線に対する感度は低い。この欠点を解消するために、フォトダイオードＰＤのｎ＋領域を深くまで形成できる横型オーバーフロードレイン（ＬＯＤ）電極を有するＦＴ－ＣＣＤについて次に説明する。

【００５１】

（実施の形態４）

図２０は横型オーバーフロードレイン（ＬＯＤ）電極を有するフレーム・トランスファ型ＣＣＤ（ＦＴ－ＣＣＤ）の構成を示している。図２０の破線で囲まれた部分は１画素分のフォトダイオードＰＤを構成しており、その断面構造を図２１に示す。ｐ型基板４２の表面には、フォトダイオードとなるｎ型領域４５を深く形成できるように、エピタキシャル成長によりｐ型領域４２’が形成されている。フォトダイオードとなるｎ型領域４５を深く形成できることにより、近赤外光に対する感度を高くできる特徴がある。フォトダイオードとなるｎ型領域４５に隣接してｐ＋領域４４が形成されており、このｐ＋領域４４に横型オーバーフロードレインとなるｎ型領域４０が形成されている。フォトダイオードとなるｎ型領域４５と横型オーバーフロードレインとなるｎ型領域４０は、隣接して基板の垂直転送方向に長く延びており、各ｎ型領域４０はアルミニウム電極よりなる横型オーバーフロードレイン（ＬＯＤ）電極４１に接続されている。ＬＯＤ電極４１には制御電圧Ｖｓが印加されている。

【００５２】

ｎ型領域４５の表面には、SiO_2 よりなる絶縁薄膜４６を介して、ｎ型領域４５の長手方向に沿って複数個のポリシリコンゲート電極ａ，ｂ，ｃが形成されている。各ポリシリコンゲート電極ａ，ｂ，ｃはｎ型領域４５の長手方向とは垂直方向に伸びるように形成されており、３個のゲート電極ａ，ｂ，ｃで一つの画素を構成している。図２０では限られた個数の画素しか図示していないが、実際には水平方向および垂直方向の解像度に応じた個数の画素が構成されるものである。

【００５３】

ポリシリコンゲート電極ａ，ｂ，ｃおよびSiO_2 よりなる絶縁薄膜４６は光を透過するので、ｎ型領域４５には光電子が発生する。ただし、図２０の撮像部以外の部分は遮光膜で覆われており、蓄積部や水平転送部には光電子は発生しない。蓄積部は垂直帰線期間中に撮像部の信号電荷を一括して高速転送され、蓄積部に蓄積された信号電荷を次回の垂直帰線期間までの間に水平転送部を介して読み出すものである。蓄積部のゲート電極に印加される電圧φ１～φ３は撮像部のゲート電極に印加される電圧Ｖ１～Ｖ６とは分離されており、蓄積部から水平転送部を介して画像信号を読み出している途中においても撮像部において信号電荷の蓄積が可能である。したがって、フレーム・トランスファ型ＣＣＤを用いると、インターライン・トランスファ型ＣＣＤを用いる場合に比べて同期積分の蓄積時間を長く取ることが可能となる。この例では、Ｖ１～Ｖ６の６相の転送電圧を用いて撮像部から蓄積部に信号電荷を転送可能としている。一方、蓄積部から水平転送部には、φ１～φ３の３相の転送電圧を用いて信号電荷を転送可能としている。（撮像部および蓄積部の各ゲート電極は、水平方向に並んだ電極に同じ転送電圧Ｖ１～Ｖ６、φ１～φ３が印加されるように図示しない配線を介して接続されている。）水平転送部は上述した水平転送ＣＣＤと同じものであるので、詳細な説明は省略するが、ここでもＶＨ１，ＶＨ２の２相の転送電圧を用いて信号電荷を転送可能としている。

【００５４】

図２２は図２１の破線に沿って電子のポテンシャルを示している。光電子が発生するｎ型領域４５とこれにｐ＋領域４４を介して隣接するｎ型領域４０の間には、図２２の破線で示すように、ｐ＋領域４４による電位障壁が存在するが、ｎ型領域４０に接続されたＬＯＤ電極４１に高い＋電圧を印加すると、この電位障壁を崩すことができ、ｎ型領域４５からｎ型領域４０を経てＬＯＤ電極４１に信号電荷（光電子）を捨てることができる。

【００５５】

光電子の蓄積期間では、ＬＯＤ電極４１の印加電圧Ｖｓは低くしておき、ｎ型領域４５とｎ型領域４０の間に、ｐ＋領域４４による電位障壁が存在するようにしておく。また、図２３（イ）のように、１画素につき３枚のゲート電極ａ，ｂ，ｃを使用し、中央のゲート電極ｂに最も高い＋電圧を印加することでゲート電極ｂ下で発生した光電子のみならずゲート電極ａ、ｃ下で発生した光電子もゲート電極ｂ下のポテンシャル井戸に蓄積する。この様子を図２３（ハ）に示す。図２３（ハ）は図２３（イ）の太い一点鎖線についての電子のポテンシャルを示したものである。また、図２３（ニ）は図２３（ロ）の太い破線についての電子のポテンシャルを各ゲート電極ａ，ｂ，ｃについて示している。

【００５６】

光電子の廃棄期間では、ＬＯＤ電極４１に高い＋電圧を印加し、図２３（ニ）に示すように、ｎ型領域４５とｎ型領域４０の間のｐ＋領域４４による電位障壁の高さを下げる。このとき、ＬＯＤ電極４１に印加する電圧Ｖｓは、ｎ型領域４０のポテンシャルがゲート電極ｂ下のｎ型領域４５のポテンシャルよりも高く、且つゲート電極ａ、ｃ下のｎ型領域４５のポテンシャルよりも低くなるように設定する。ゲート電極ａ，ｂ，ｃに印加される電圧は、光電子の蓄積期間と同様であり、中央のゲート電極ｂには両側のゲート電極ａ，ｃよりも高い＋電圧が印加されているので、両側のゲート電極ａ，ｃの下ではｐ＋領域４４による電位障壁は完全に崩されるが、中央のゲート電極ｂの下ではｐ＋領域４４による電位障壁は高さが低くなるだけで完全には崩されない。このため、両側のゲート電極ａ，ｃの下で発生した光電子の多くはｎ型領域４０に廃棄されるが、中央のゲート電極ｂの下で発生した光電子は廃棄されないし、光電子の蓄積期間において中央のゲート電極ｂの下に

蓄積された光電子も廃棄されない。

【００５７】

上述の光電子の蓄積と廃棄を複数回繰り返すと、中央のゲート電極ｂの下には、光電子の蓄積期間において両側のゲート電極ａ，ｂから中央のゲート電極ｂに蓄積された光電子が余分に蓄積されることになる。中央のゲート電極ｂは常に光電子を蓄積しているので、この常時積分による平均値が同期積分による検出値に加算されることになるが、それでも両側のゲート電極ａ，ｂから同期積分による検出値を得ているので、十分なコントラストを得ることができる。

【００５８】

図１６～図２３に示した実施の形態３，４では、３枚のゲート電極で１画素を構成する場合について説明したが、図２４や図２５に示すように、４枚以上のゲート電極で１画素を構成する場合には、電荷を廃棄する期間に、光電子を蓄積しているゲート電極に周囲から光電子が流入しないように、電位障壁を形成すると良い。図２４は４枚のゲート電極で１画素を構成する場合、図２５は６枚のゲート電極で１画素を構成する場合であり、（ａ）は電荷蓄積期間、（ｂ）は電荷廃棄期間における各ゲート電極下の電子のポテンシャルを示している。図２４、図２５において灰色で示した部分は光電子であり、（ａ）の電荷蓄積期間では、電子のポテンシャルが最も低いゲート電極下に周囲のゲート電極下で発生した光電子が流入して蓄積され、（ｂ）の電荷廃棄期間では、電子のポテンシャルが最も低いゲート電極下の光電子が蓄積された部分を周囲から電気的に孤立させるように、隣接するゲート電極下に電位障壁を形成するように制御している。

【００５９】

図２５に示した６枚のゲート電極で１画素を構成する場合について、電荷蓄積期間と電荷廃棄期間における各ゲート電極下の電子のポテンシャルを３次元的に示すと、図２７（ａ），（ｂ）のようになる。図中のＶ１～Ｖ６は図２０に示した垂直転送電圧に対応しており、ＬＯＤは横型オーバーフロードレインとなるｎ型領域４０に対応している。図２７（ａ）の電荷蓄積期間では、Ｖ２，Ｖ６の電圧を印加されたゲート電極下の光電子がＶ３，Ｖ５の電圧を印加されたゲート電極下に移動すると共に、Ｖ３，Ｖ５の電圧を印加されたゲート電極下の光電子はＶ４の電圧を印加されたゲート電極下に移動し、このＶ４の電圧を印加されたゲート電極下に光電子が蓄積される。図２７（ｂ）の電荷廃棄期間では、Ｖ３，Ｖ５の電圧をＶ１と同程度まで低くすることで、Ｖ４の電圧を印加されたゲート電極下の光電子が蓄積された部分は周囲から電気的に孤立し、光電子の流入は阻止される。また、ＬＯＤ電極の電子のポテンシャルを、Ｖ４の電圧を印加されたゲート電極よりも高く、且つＶ２，Ｖ６の電圧を印加されたゲート電極よりも低く設定することにより、Ｖ４の電圧を印加されたゲート電極下に蓄積された光電子は廃棄することなく、Ｖ２，Ｖ６の電圧を印加されたゲート電極下で発生した光電子はＬＯＤ電極に廃棄される。

【００６０】

ところで、図２５の例では、非検知位相の光電子の一部はＶ４の電圧を印加された蓄積用電極部（電子のポテンシャルが最も深い位置の電極）に流入する。また、蓄積用電極部自身も、非検出位相の光電子を発生し蓄積する。これら非検出位相の光電子は、検出位相の光電子に対してＤＣ成分となり、Ｓ／Ｎ比を低下させる。そこで、図２６に示すように、電荷蓄積用の感光部と電位障壁を形成する感光部の表面に遮光膜４７を設ければ、同期積分に対する常時積分の比率を低減でき、同期積分のコントラストを改善できる。図２６の例では、Ｖ２，Ｖ６の電圧を印加されるゲート電極下にのみ光電子が発生するように、Ｖ１，Ｖ３，Ｖ４，Ｖ５の電圧を印加されるゲート電極の表面を遮光膜４７で覆っている。

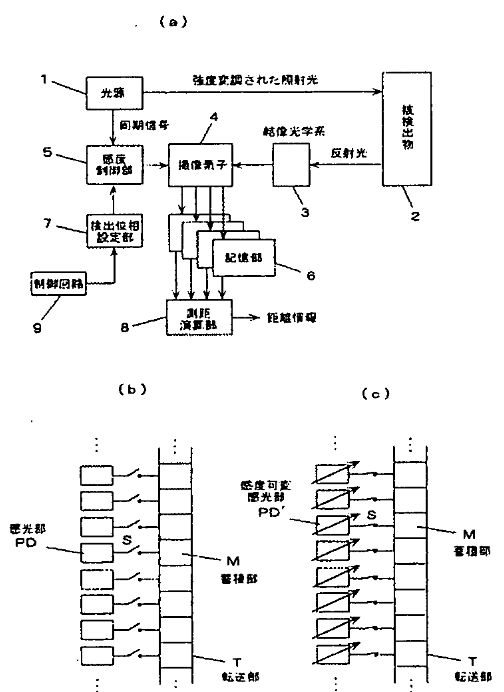
【００６１】

なお、本発明はＩＴ－ＣＣＤやＦＴ－ＣＣＤに限らず、これらの複合型であるＦＩＴ－ＣＣＤ（フレーム・インターライン・トランスファ型ＣＣＤ）でも同様に適用できる。ＦＩＴ－ＣＣＤは、図２８に示すように、ＩＴ－ＣＣＤの水平転送部と撮像部の間に１画面分の蓄積部を追加したものであり、垂直転送電圧が２種類必要となり、動作は複雑になるが、ＩＴ－ＣＣＤの欠点であるスミアを低減できる利点がある。

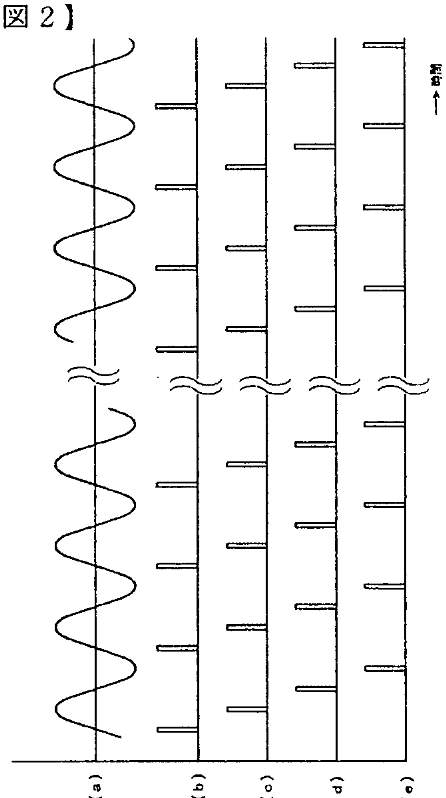
【００６２】
【発明の効果】
請求項１の発明によれば、強度変調された照射光に同期して感光部の感度を可変としたので、簡単な構成で光波測距を実現できる。
請求項２の発明によれば、強度変調された照射光に同期して感光部の感度を可変としたので、感光部から蓄積部への信号電荷の移送を高周波で開閉できる電気スイッチが必要なく、同期積分以外の用途の撮像素子でも利用可能である利点がある。
請求項３の発明によれば、ＣＣＤ撮像素子として最も一般的な縦型オーバーフロードレイン電極を有するインターライン・トランスファ型ＣＣＤ撮像素子を用いて同期積分と同じような動作を実現可能としたので、特殊な撮像素子を用いずに安価に光波測距を実現できる。
【００６３】
請求項４または６の発明によれば、近赤外光に対する感度の高い横型オーバーフロードレイン電極を有するＣＣＤ撮像素子を用いて同期積分と同じような動作を実現可能としたので、暗視性能の高い測距が可能となる。
請求項５または６の発明によれば、フレーム・トランスファ型ＣＣＤを用いているので、インターライン・トランスファ型ＣＣＤを用いる場合に比べて同期積分の蓄積時間を長く取ることが可能となる。
【００６４】
請求項７の発明によれば、電荷廃棄期間では、電荷蓄積用の感光部を他の感光部から電気的に孤立させる電位障壁を形成するようにしたので、同期積分のコントラストを改善できる。
請求項８の発明によれば、電荷蓄積用の感光部と電位障壁を形成する感光部の表面に遮光部を設けたので、同期積分に対する常時積分の比率を低減でき、同期積分のコントラストを改善できる。
請求項９の発明によれば、感光部から蓄積部への信号電荷の移送を高周波で開閉できる電気スイッチを各センサ要素ごとに設けているので、検出位相の信号電荷のみを選択的に蓄積することができるから、同期積分のコントラストを改善できる。
請求項１０の発明によれば、蓄積部を転送部として兼用するために設けられた転送電極を感光部から蓄積部への信号電荷の移送を高周波で開閉するための電気スイッチとしてさらに兼用したので、簡単な構成で同期積分の動作を実現できる。
【図面の簡単な説明】
【図１】本発明の基本構成を示す説明図であり、（ａ）は全体構成を示すブロック図、（ｂ）は撮像素子の一例を示す要部構成図、（ｃ）は撮像素子の他の一例を示す要部構成図である。
【図２】本発明の撮像素子による同期積分のタイミングを示す動作説明図である。
【図３】従来の光波測距に用いる光学系の概略構成図である。
【図４】従来の光波測距の原理説明図である。
【図５】従来の光波測距に用いる撮像素子の一例を示す要部構成図である。
【図６】従来の光波測距に用いる撮像素子の他の一例を示す要部構成図である。
【図７】本発明の実施の形態１の撮像素子の全体構成を示す平面図である。
【図８】本発明の実施の形態１の撮像素子の要部構成を示す斜視図である。
【図９】本発明の実施の形態１の撮像素子の要部構成を示す断面図である。
【図１０】本発明の実施の形態１の撮像素子の電子のポテンシャルを示す説明図である。
【図１１】本発明の実施の形態１の撮像素子の動作説明図である。
【図１２】本発明の実施の形態２の撮像素子の全体構成を示す平面図である。
【図１３】本発明の実施の形態２の撮像素子の要部構成を示す斜視図である。
【図１４】本発明の実施の形態２の撮像素子の電子のポテンシャルを示す説明図である。
【図１５】本発明の実施の形態２の撮像素子の動作説明図である。
【図１６】本発明の実施の形態３の撮像素子の全体構成を示す平面図である。

【図１７】本発明の実施の形態３の撮像素子の要部構成を示す斜視図である。
【図１８】本発明の実施の形態３の撮像素子の電子のポテンシャルを示す説明図である。
【図１９】本発明の実施の形態３の撮像素子の動作説明図である。
【図２０】本発明の実施の形態４の撮像素子の全体構成を示す平面図である。
【図２１】本発明の実施の形態４の撮像素子の要部構成を示す斜視図である。
【図２２】本発明の実施の形態４の撮像素子の電子のポテンシャルを示す説明図である。
【図２３】本発明の実施の形態４の撮像素子の動作説明図である。
【図２４】４相のゲート電圧を用いたＦＴ－ＣＣＤの動作を示す説明図である。
【図２５】６相のゲート電圧を用いたＦＴ－ＣＣＤの動作を示す説明図である。
【図２６】６相のゲート電圧を用いたＦＴ－ＣＣＤの感光部に遮光膜を付加した場合の動作を示す説明図である。
【図２７】６相のゲート電圧を用いたＦＴ－ＣＣＤの動作を３次元的に示す説明図である。
【図２８】ＦＩＴ－ＣＣＤの全体構成を示す平面図である。
【符号の説明】
1　光源
2　被検出物
3　結像光学系
4　撮像素子
5　感度制御部
6　記憶部
7　検出位相設定部
8　測距演算部

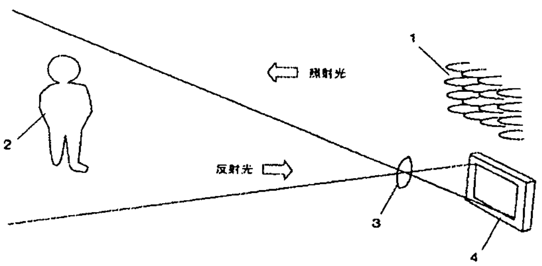
【図１】



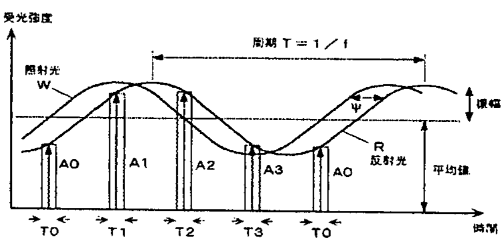
【図２】



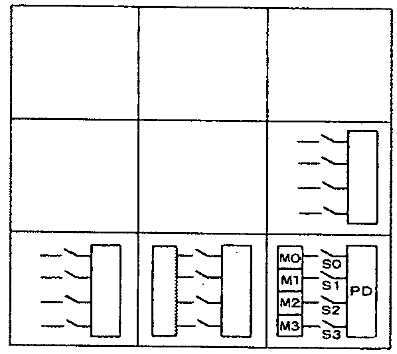
【図３】



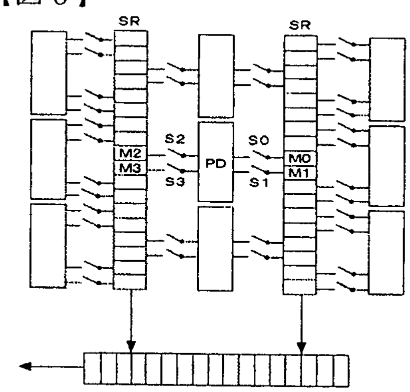
【図４】



【図５】



【図６】



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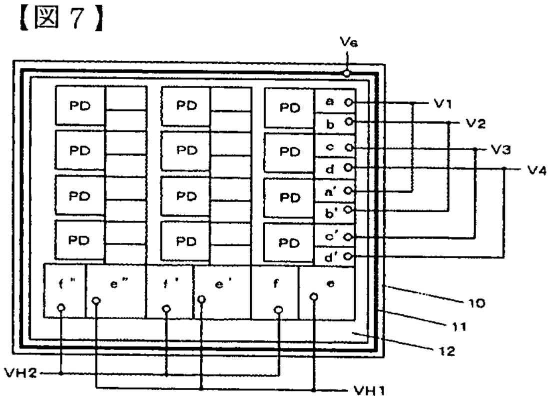

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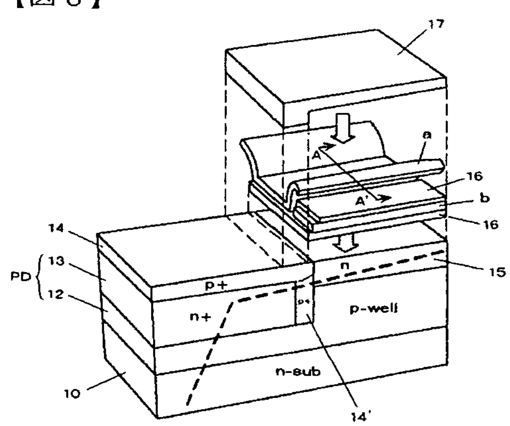

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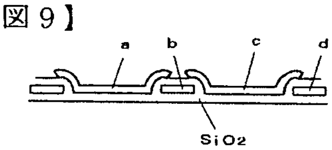
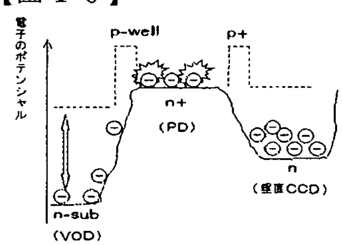
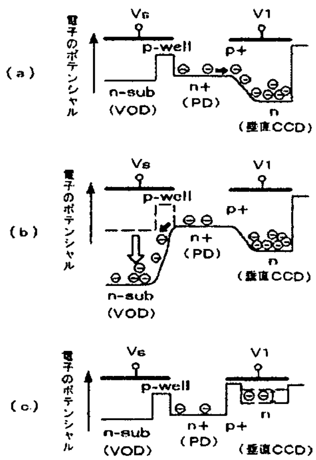


【図１０】



【図１１】



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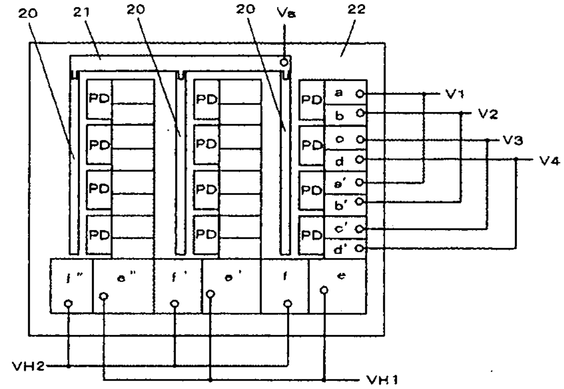

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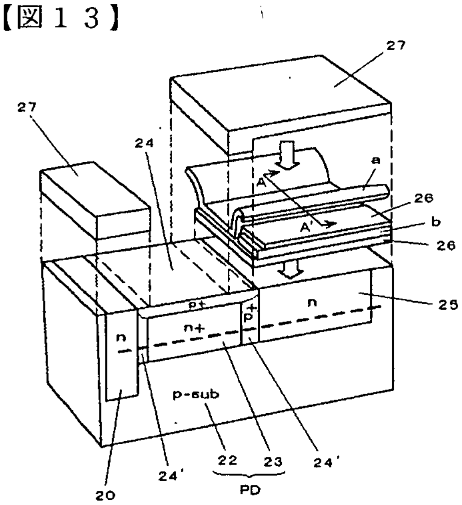

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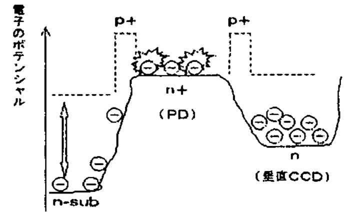

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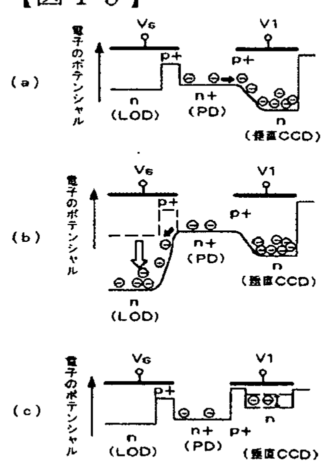

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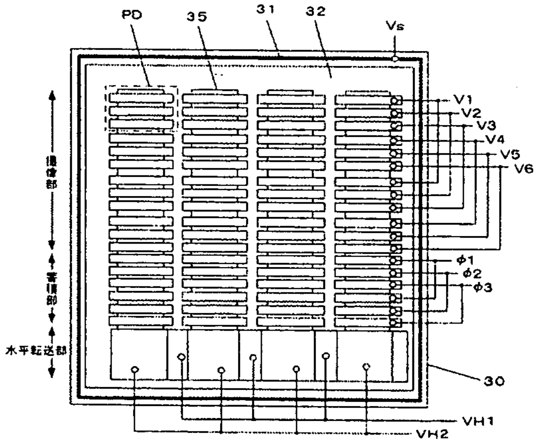
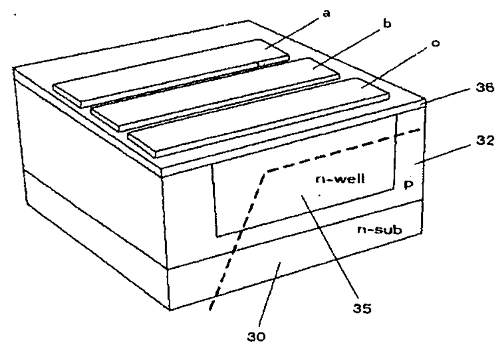


【図１７】



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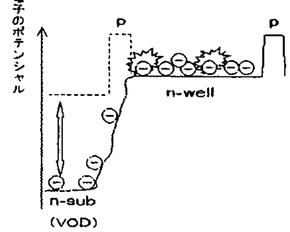
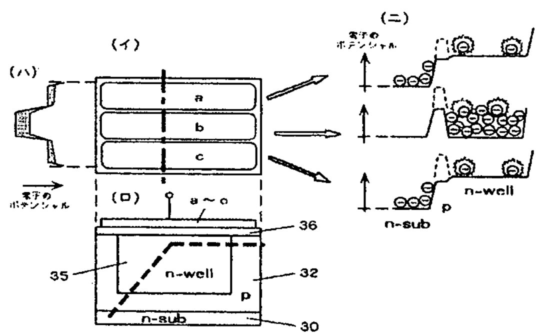
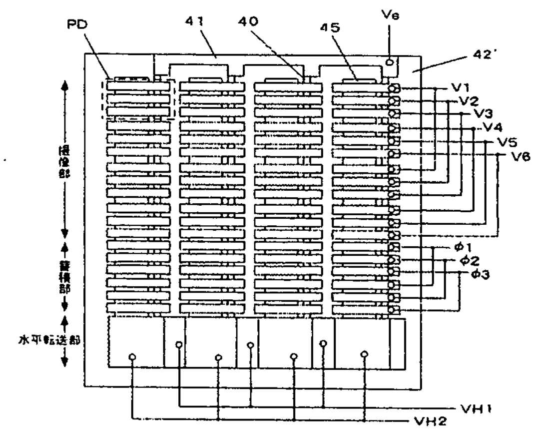


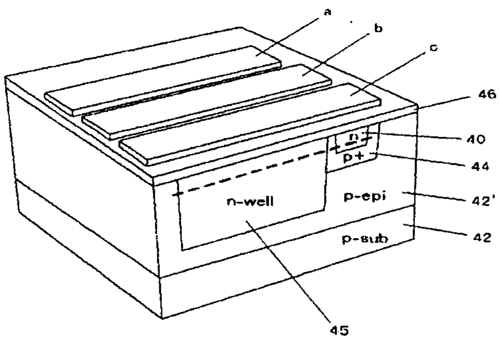
【図１９】



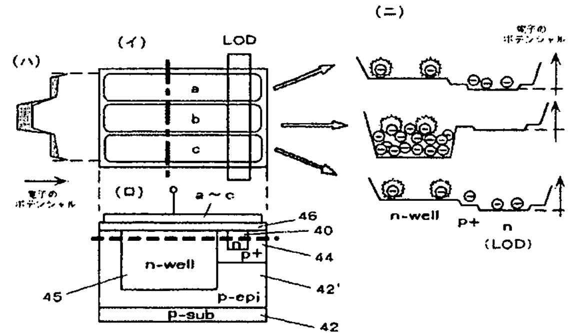
【図２０】



【図２１】



【図２３】



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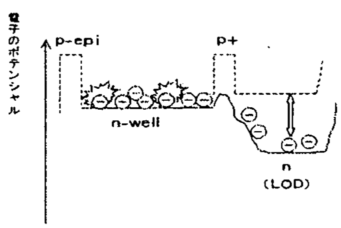
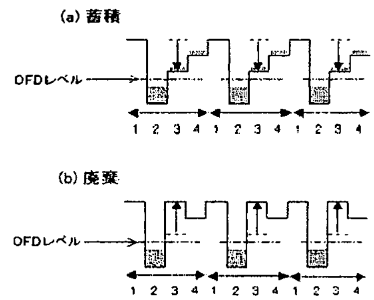
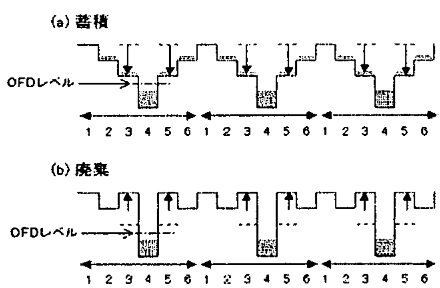


【図２４】



【図２５】



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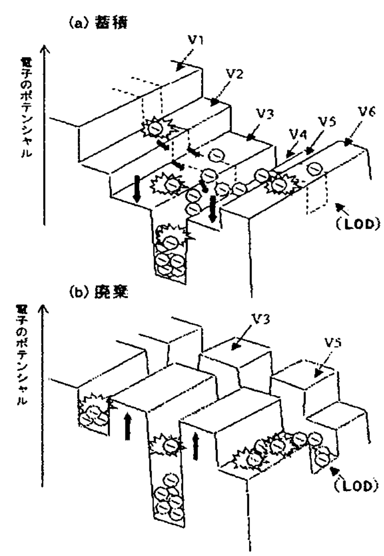
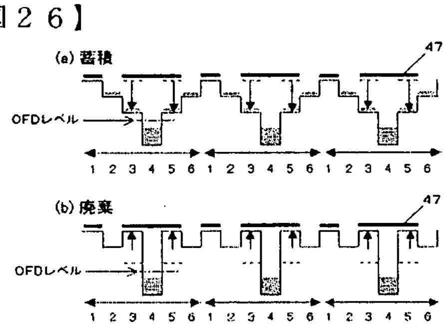
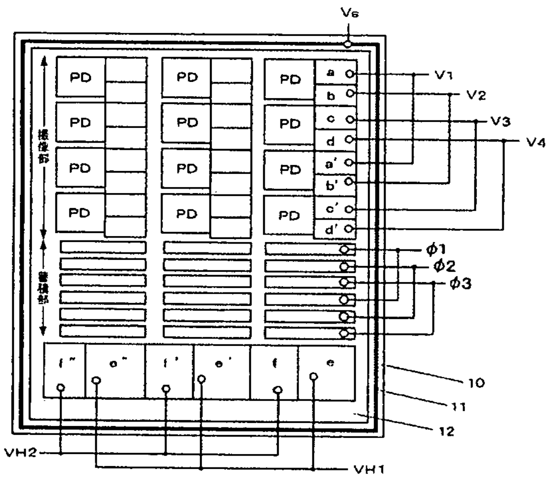


【図２６】



【図２８】


Vs
PD
a
b
c
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a'
b'
c'
d'
V1
V2
V3
V4
撮像部
蓄積部
φ1
φ2
φ3
f"
e"
f'
e'
f
e
10
11
12
VH2
VH1

フロントページの続き

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FA24
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